Multifunctional nanoscale oxide conductors and semiconductors

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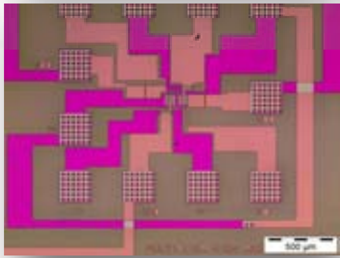
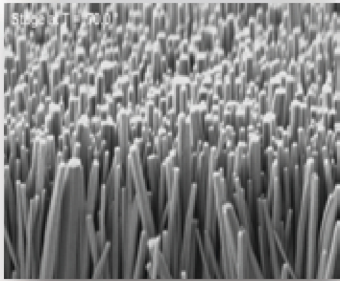
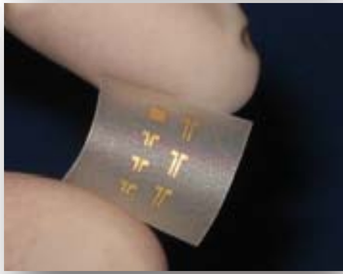






General Outline

- **Introduction**
  Transparent electronics
- **n-type TFTs by PVD**
- **n-type TFTs by solution**
- **Conclusions**
- **Other applications**

Transparent Electronics


2004

...is today a reality!

Source: YouTube – Samsung's Transparent Smart Window at CES 2012 [Official]

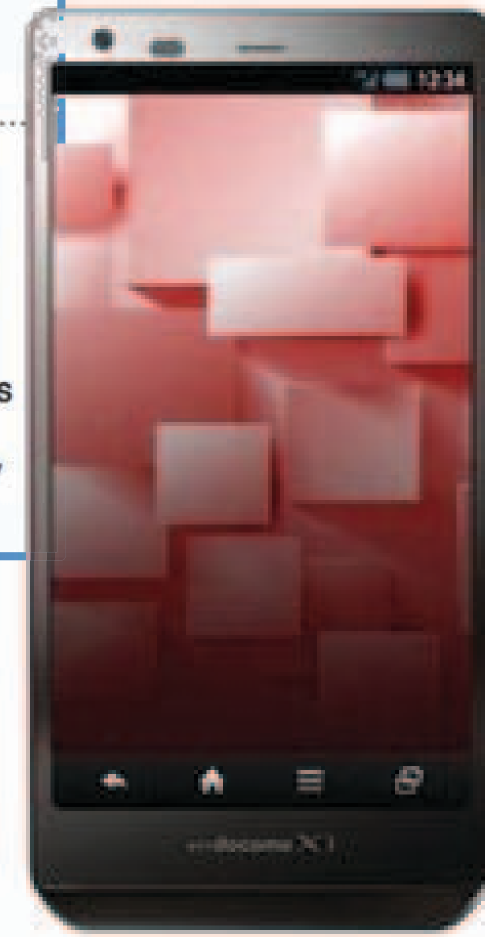
Press Release April 21, 2011

Sharp to Commercialize World's First Small- and Medium-Size LCD Panels using Oxide Semiconductor

Sharp Corporation has developed high performance small- and medium-size LCD panels using oxide semiconductor, InGaZnO (IGZO*[1]). Production of these new LCD panels will aim to start at Kameyama Plant No.2 within this year.

Meeting the strong demand for small- and medium-size LCD panels used in smart phones and tablet terminals, is accompanied by an increased need for display quality, including high resolution and high picture quality, light weight and compact design, and high energy efficiency.

1st IGZO backplane in market (4.9”, 1280x720, shipping end 2012)



Oxide TFT

Rumor?!

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best of bz

iPad 5 Likely to Use New, Lighter and Thinner Technology (AAPL)

Thursday, July 25, 2013 - 9:08am

AAPL, Apple, Digitimes, iPad 5, iPad Mini, LPL, News, Oxide TFT

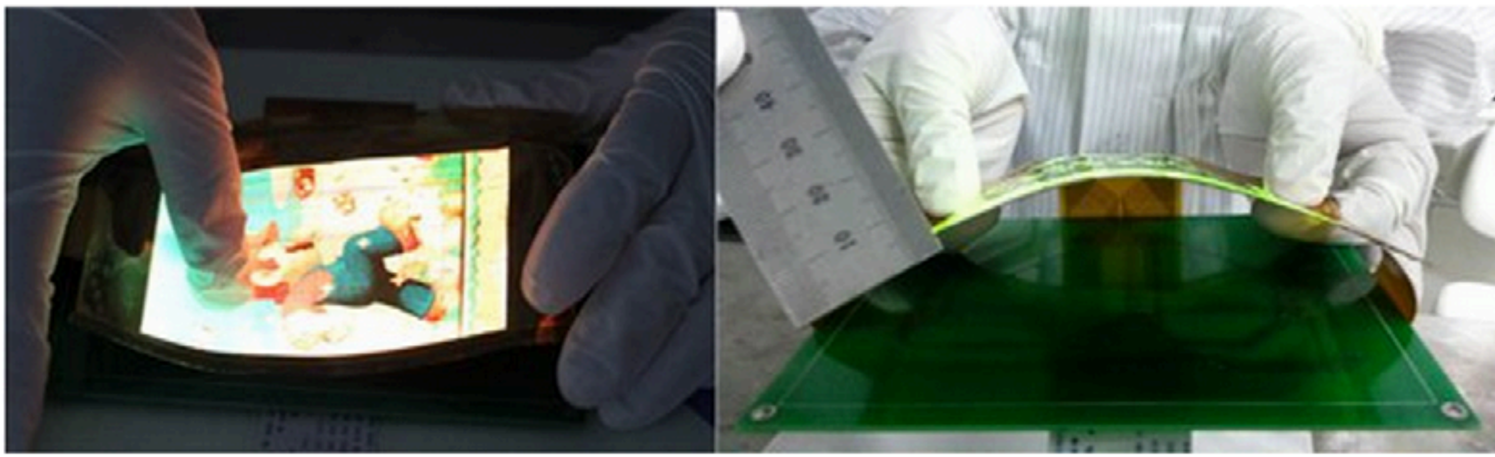
Apple's (NASDAQ: AAPL) long-awaited iPad upgrade is expected to be one of the lightest and thinnest tablets of its kind. According to DigiTimes, the fifth-generation iPad will use GF2 touch screen technology, which will allow Apple to build a lighter and thinner tablet. TPK and GIS will... **Read More >>**

OLED-Info.com

Oxide TFT News

Guangzhou New Vision developed an Ln-IZO based 4.8" flexible AMOLED panel

Guangzhou New Vision Optoelectronics (NVO) developed a flexible 4.8" AMOLED display. This full-color panel is only 100 microns thick and weighs just one gram. This panel uses an Ln-IZO backplane and a Polyimide substrate.



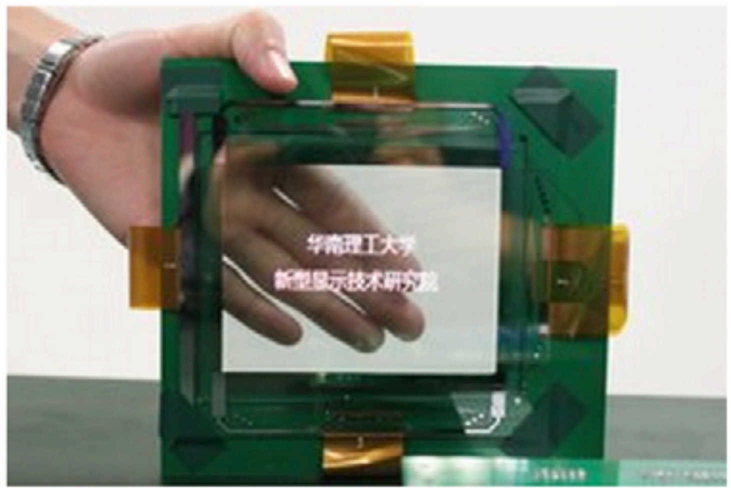
NVO developed their own Ln-IZO (Lithium-Niobate Indium-Zinc-Oxide) technology and they say that that it performs better than IGZO as it has higher electron mobility and stability and it is easier to process.

Aug 11, 2013 Read more

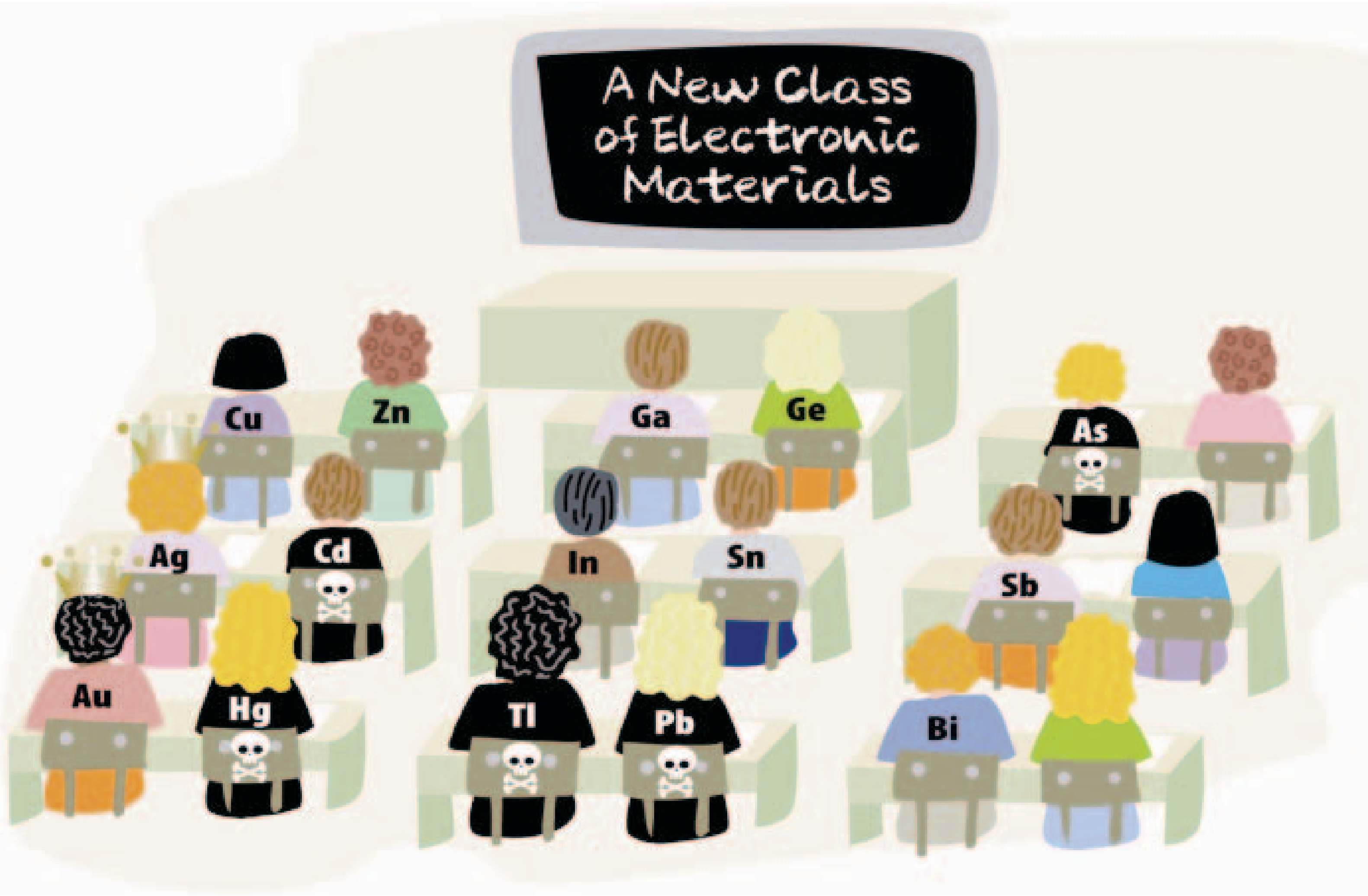
SCUT reveals new Oxide-TFT and transparent OLED prototypes

Technical / Research Transparent OLEDs OLED production Oxide TFT

The South China University of Technology (SCUT) unveiled some new AMOLED technologies: a 5" transparent AMOLED panel, an Oxide-TFT based OLED and an integrated touch AMOLED panel.




Metal oxide semiconductors

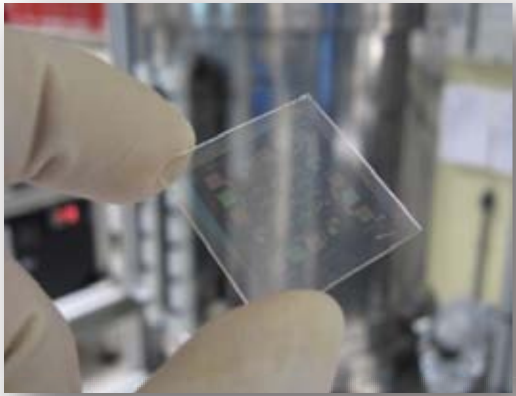

A New Class of Electronic Materials
Cu
Zn
Ga
Ge
As
Ag
Cd
In
Sn
Sb
Au
Hg
Tl
Pb
Bi

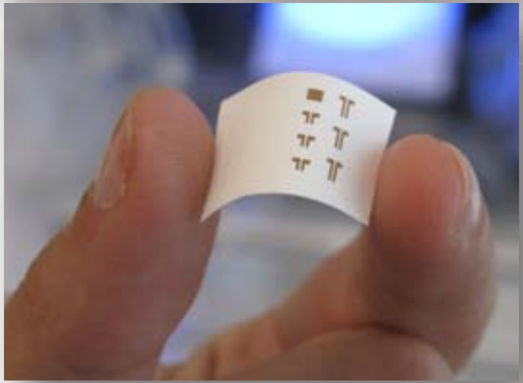
J. Wager, OSU

Why amorphous oxides are so attractive?

Main advantages

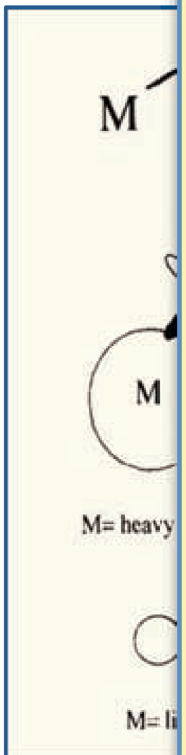
- High electrical performance (μ_{FE} & current: OLEDs)
- Enhanced stability and no visible light-degradation
- Good uniformity in large areas
- Can use the existing processing tools (sputtering)
- AOSs don't need the expensive and demanding Si crystallization processes – they are AMORPHOUS!!
- Can be produced at low temperatures, allowing to use low cost flexible substrates (even PAPER)
- Transparency.



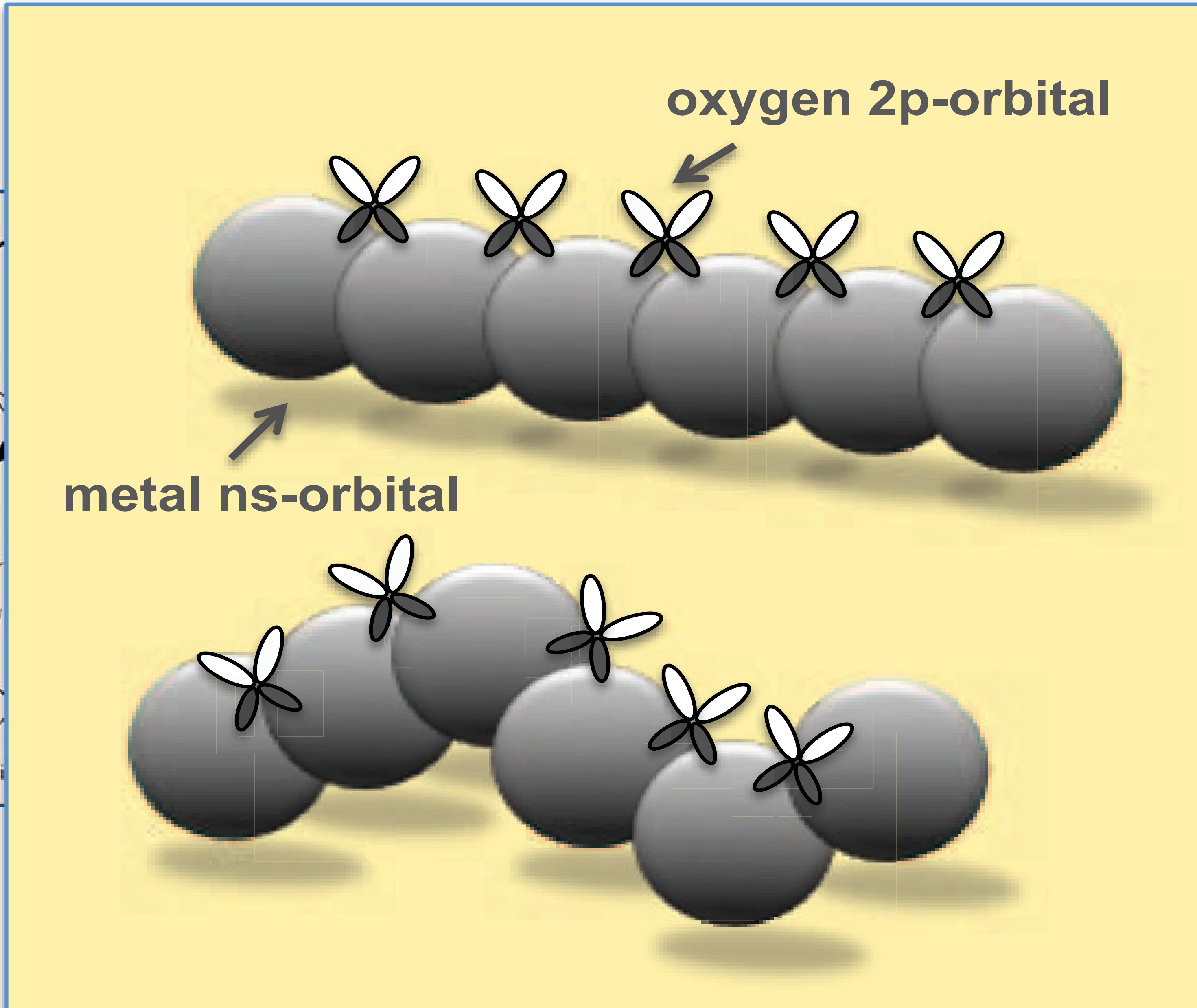


R. Martins, et al. Complementary Metal Oxide Semiconductor Technology With and On Paper, *Advanced Materials*, 23 (2011) 4491–4496.

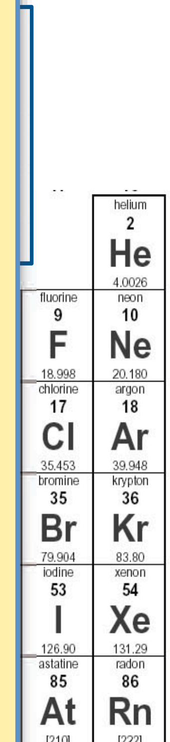
996



M
M
M= heavy
M= li

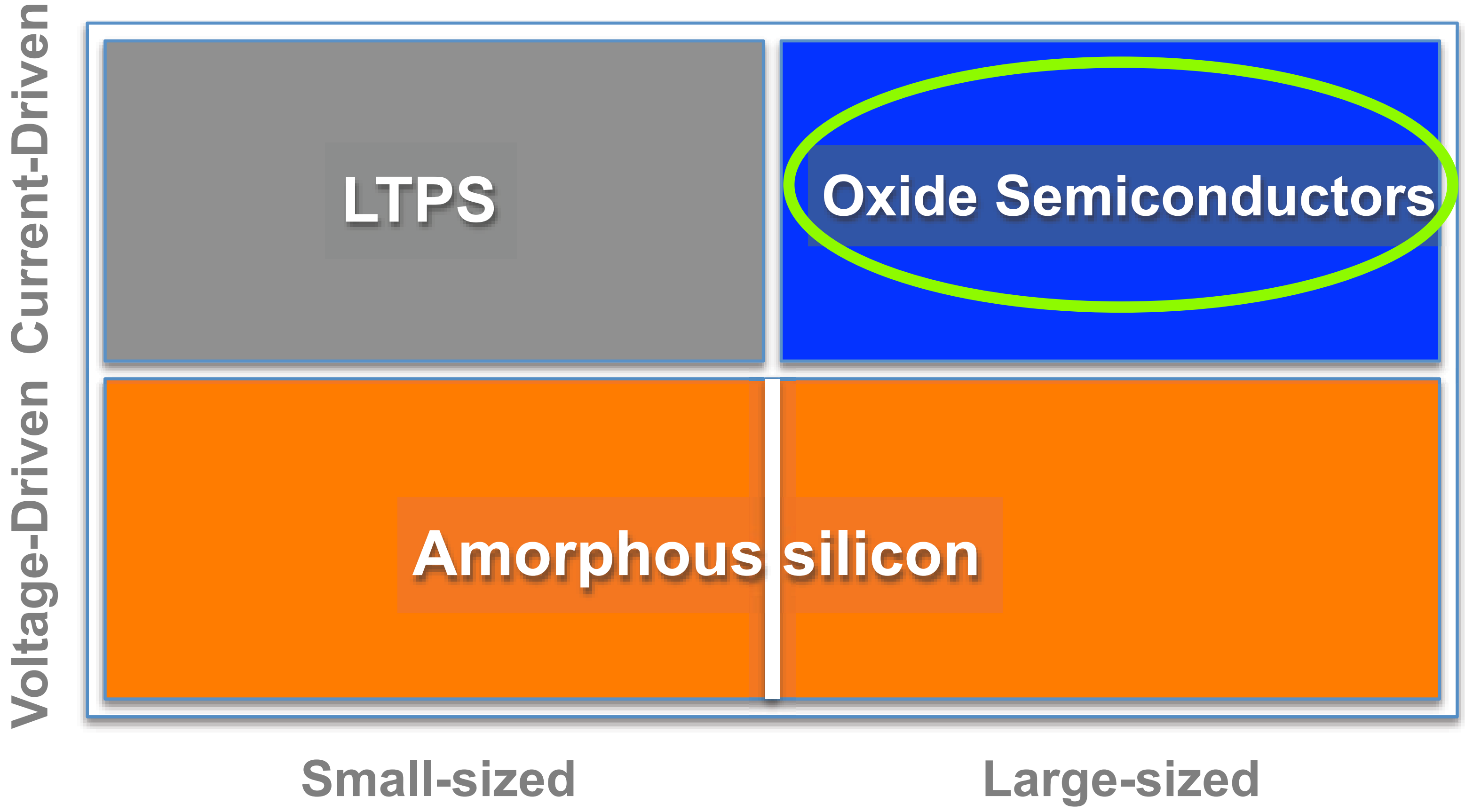


oxygen 2p-orbital
metal ns-orbital

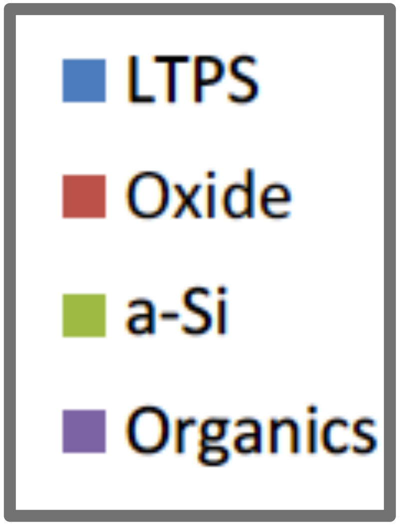


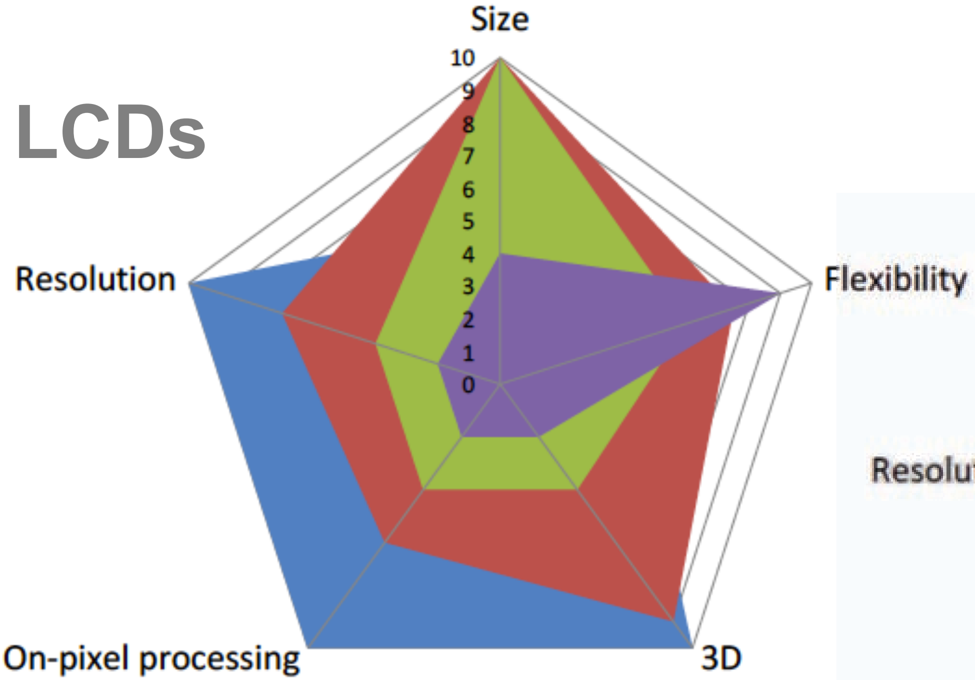
helium
2
He
4.0026
fluorine
9
F
18.998
neon
10
Ne
20.180
chlorine
17
Cl
35.453
argon
18
Ar
39.948
bromine
35
Br
79.904
krypton
36
Kr
83.80
iodine
53
I
126.90
xenon
54
Xe
131.29
astatine
85
At
[210]
radon
86
Rn
[222]

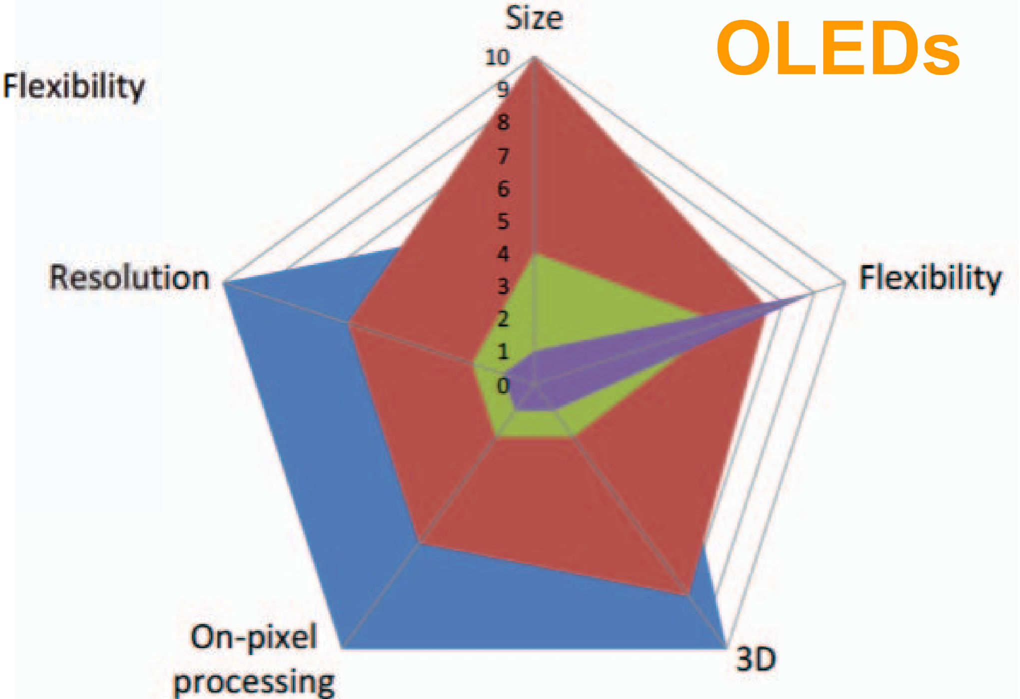
Combine simultaneously, the advantages of amorphous silicon and polycrystalline silicon TFTs



Radar chart assessing the merits of different backplane technologies



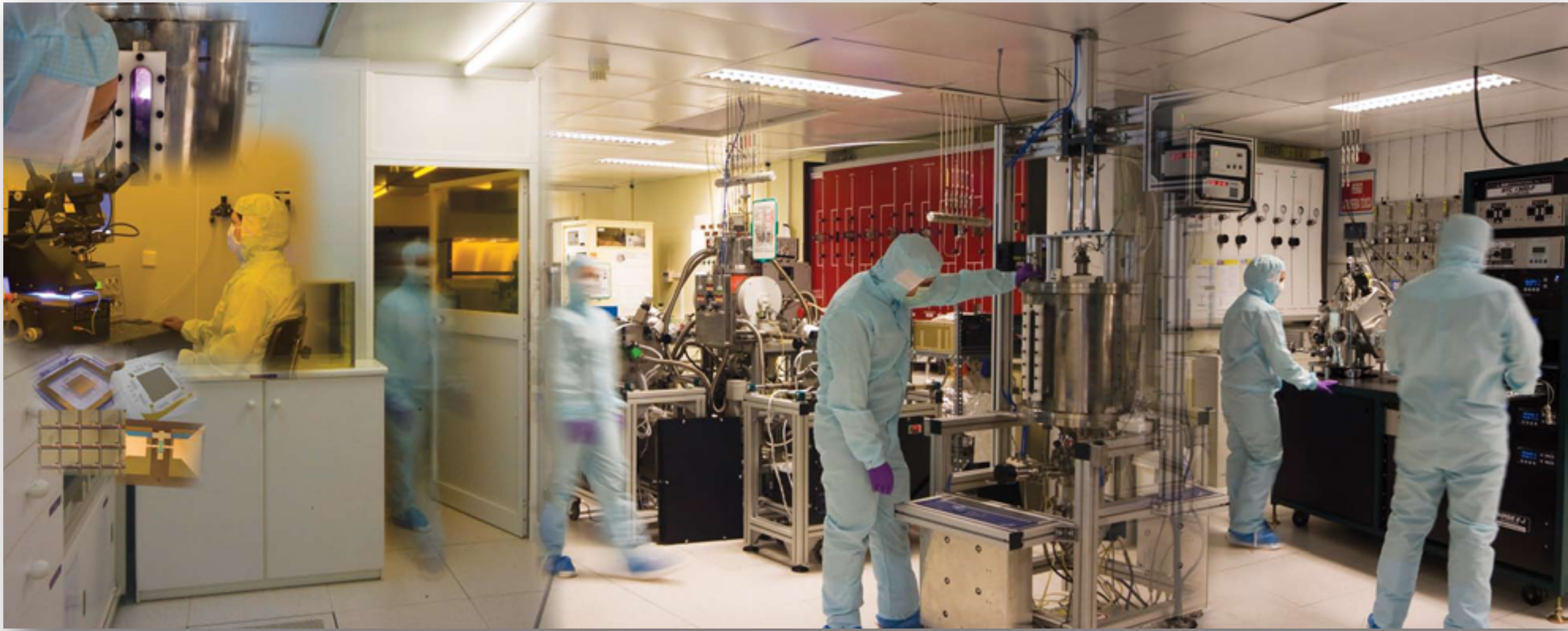




Source: www.IDTechEx.com/

n-type TFTs PVD technique @RT

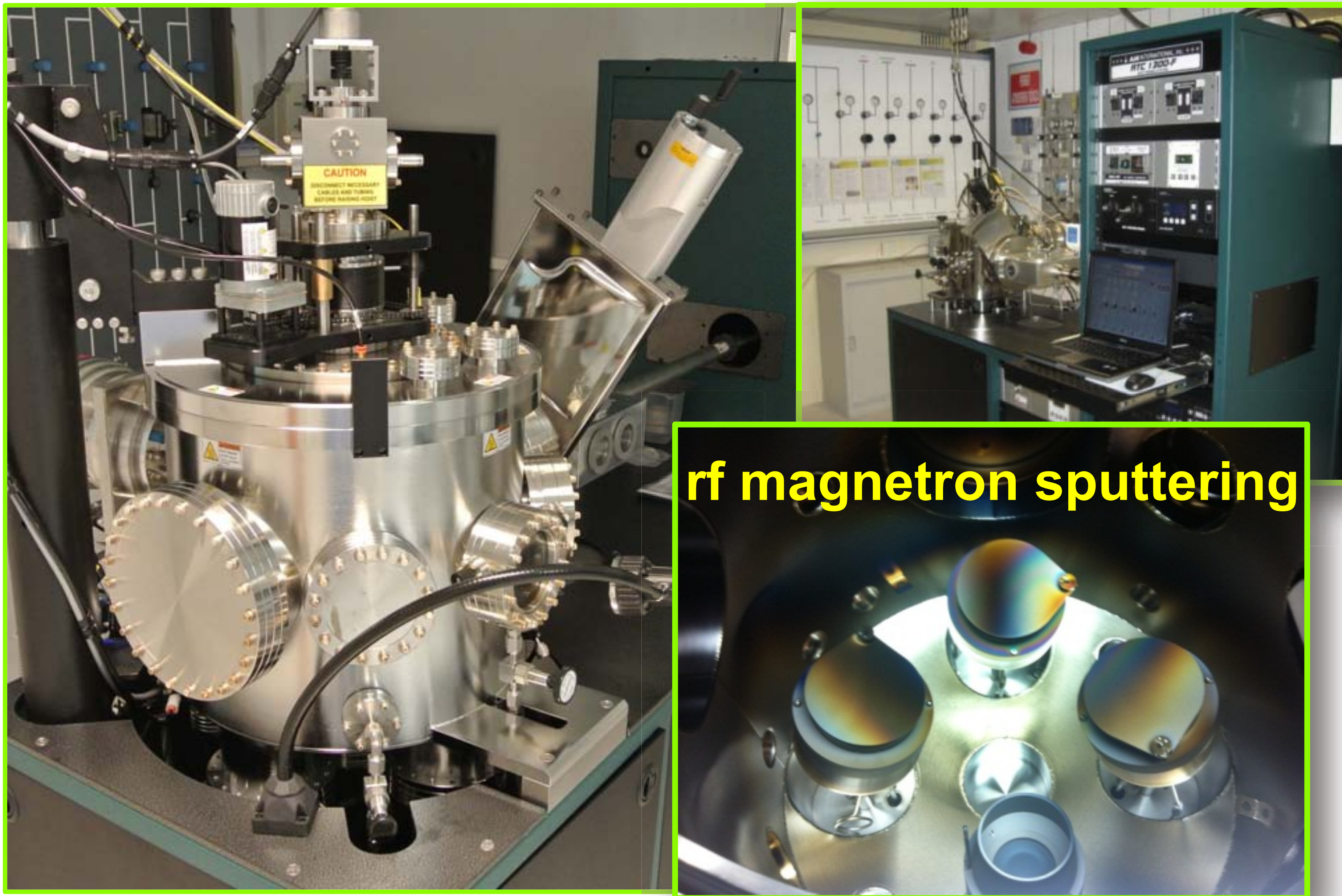
Main facilities/equipments



Two clean rooms:

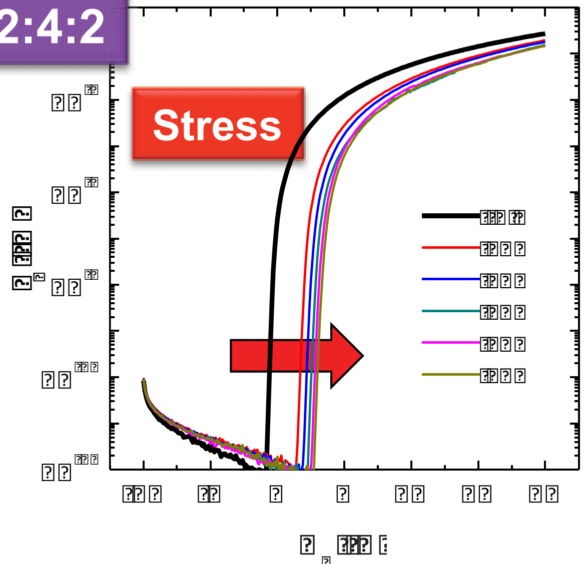
classes (1st cycle)

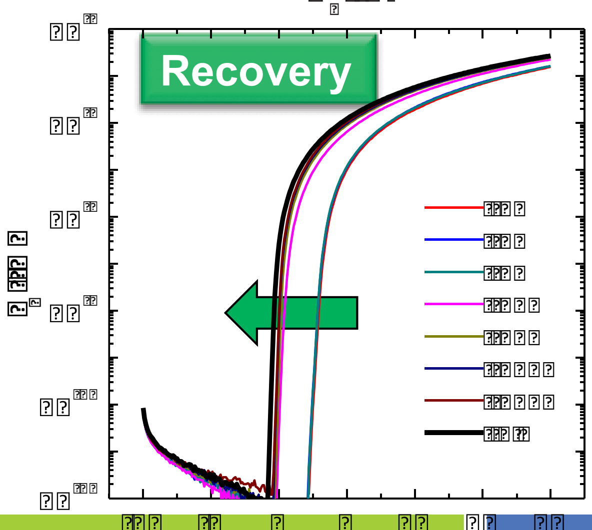
research/contracts

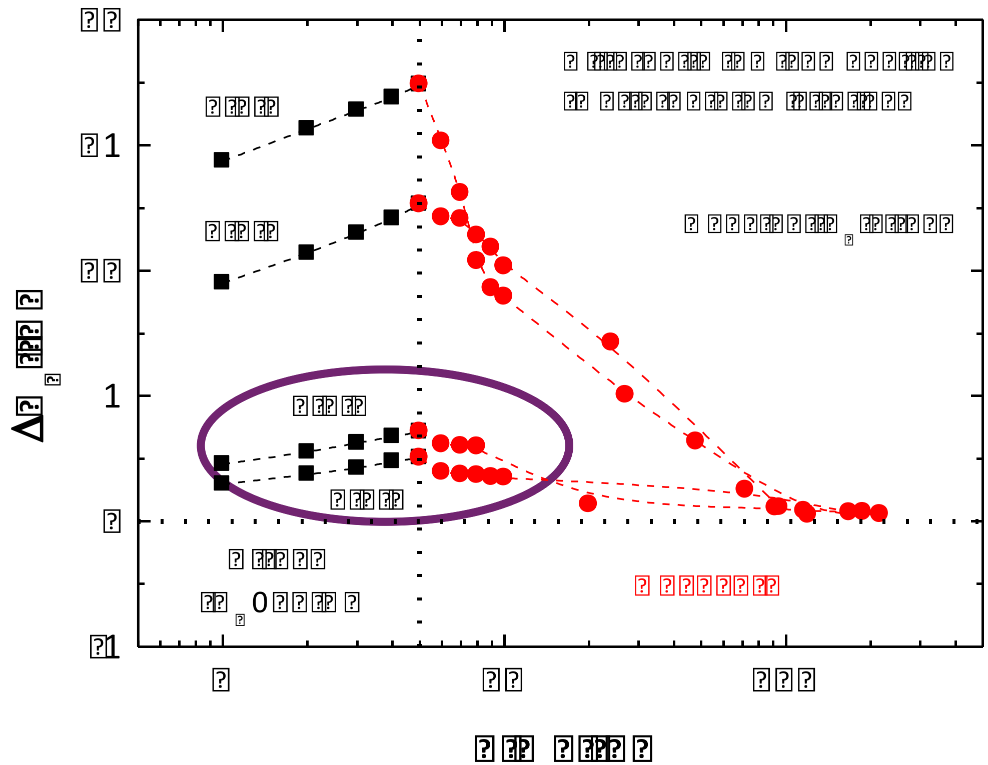

CAUTION
rf magnetron sputtering

Semiconductor composition

GIZO 2:4:2

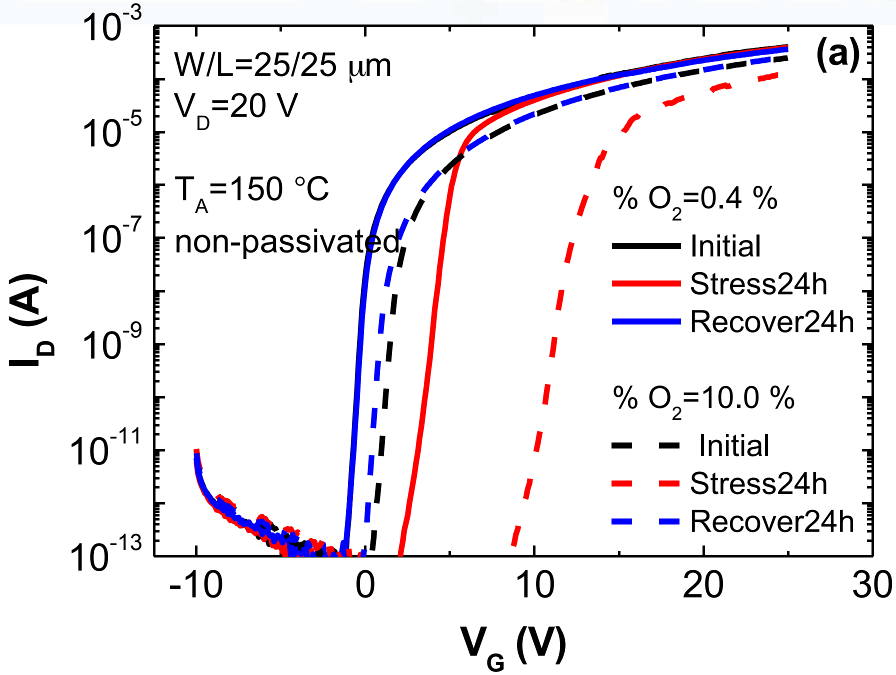


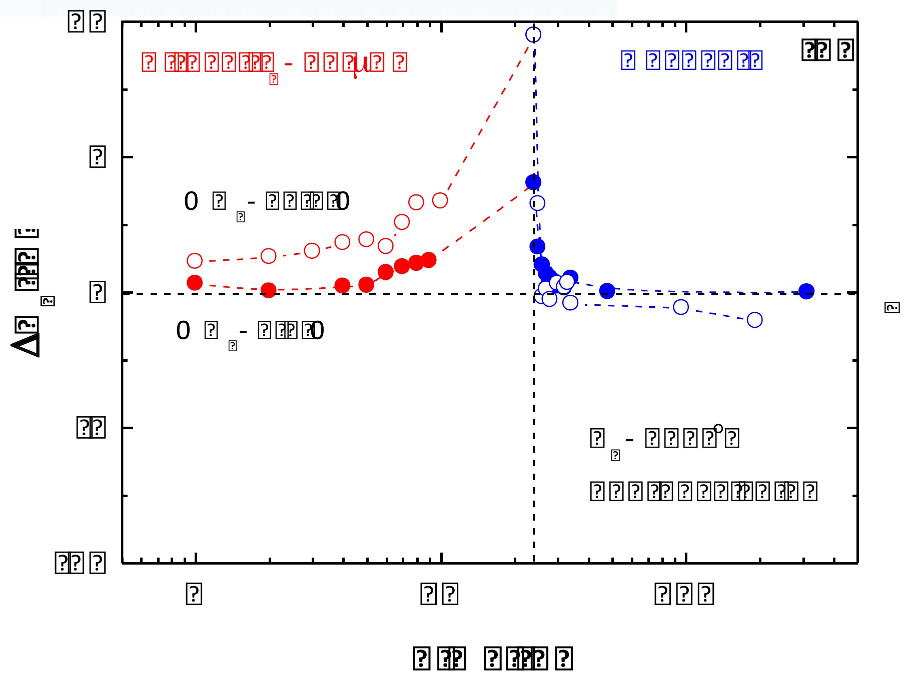




- Ga-richer compositions highly unstable under V_G stress (↓carrier concentration, ↑structural disorder close to CBM, ↑unfilled traps in the unbiased state) .
- Similar trends verified with I_D stress.

Effect of O_2 during deposition





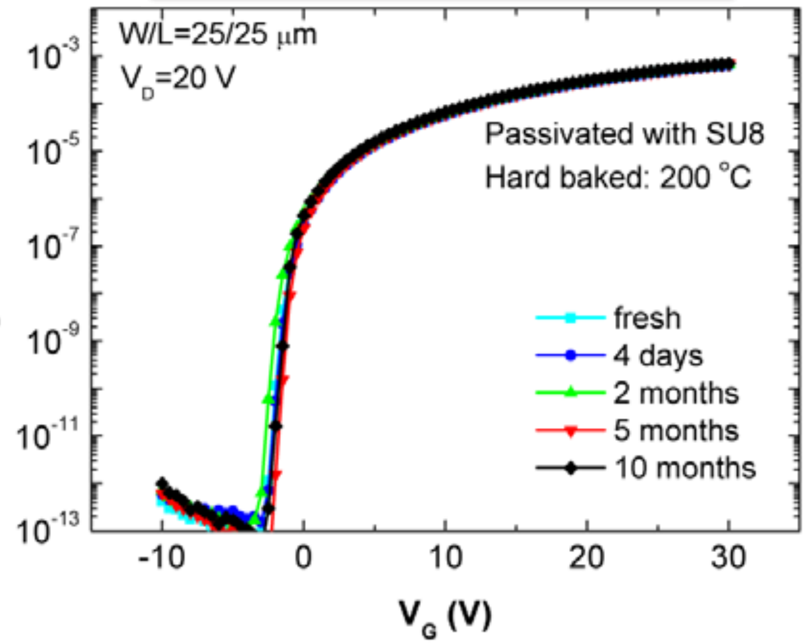
Condition	μ_{FE} (cm^2 V^{-1} s^{-1})	V_{on} (V)	S (V dec^{-1})	ΔV_{on} (V)
$\%O_2$=0.4 %, T_A=150 °C	50.1	-1.0	0.18	≈0
$\%O_2$=10.0 %, T_A=150 °C	40.8	2.0	0.29	1.5

- ΔV_T and recovery consistent with electron trapping at the semic.and/or diel./semic. Interface
- Improved performance and stability for ↓$\%O_2$

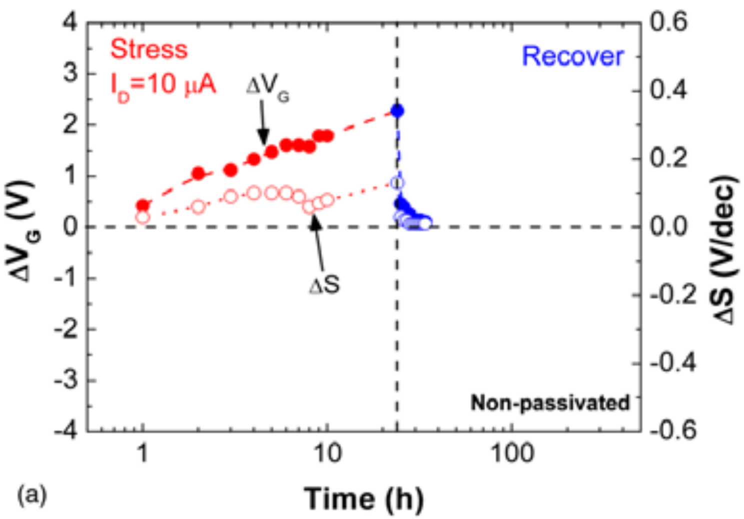
Passivation

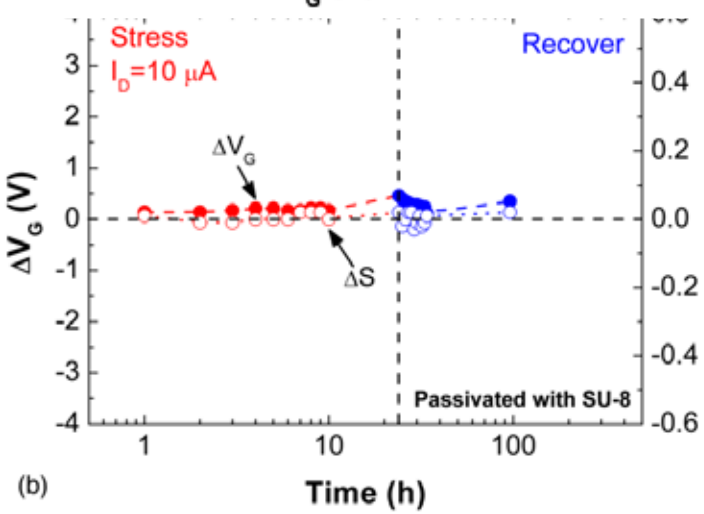
Preliminary stability measurements on SU-8 passivated devices

Stability during 10 months



Constant current stress during 24h





A. Olziersky, et al. Journal of Applied Physics, vol. 108, pp. 064505-1 – 064505-7, 2010.

Dielectric requirements

Low T processing → Sputtering → High flexibility

All TFT layers:
- Oxide semiconductor
- Dielectric
- Electrode
- Passivation layer

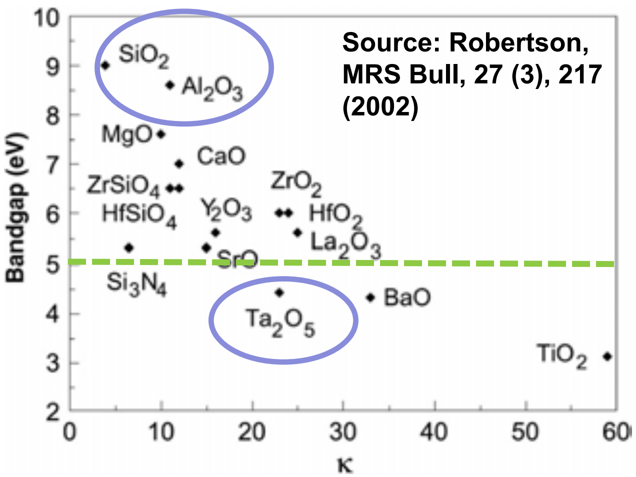
Sputtered dielectrics

- Not so good insulating properties
- Possible creation of interfacial defects

→ High k dielectrics

- Higher thickness
- Reduces interface defects influence

High-k dielectrics



Advantages

High gap (> 5 eV)

High k (20-25)

Disadvantages

Crystallization at low T

Band offset on the limit

?

High k T_2O_5

+

High bandgap

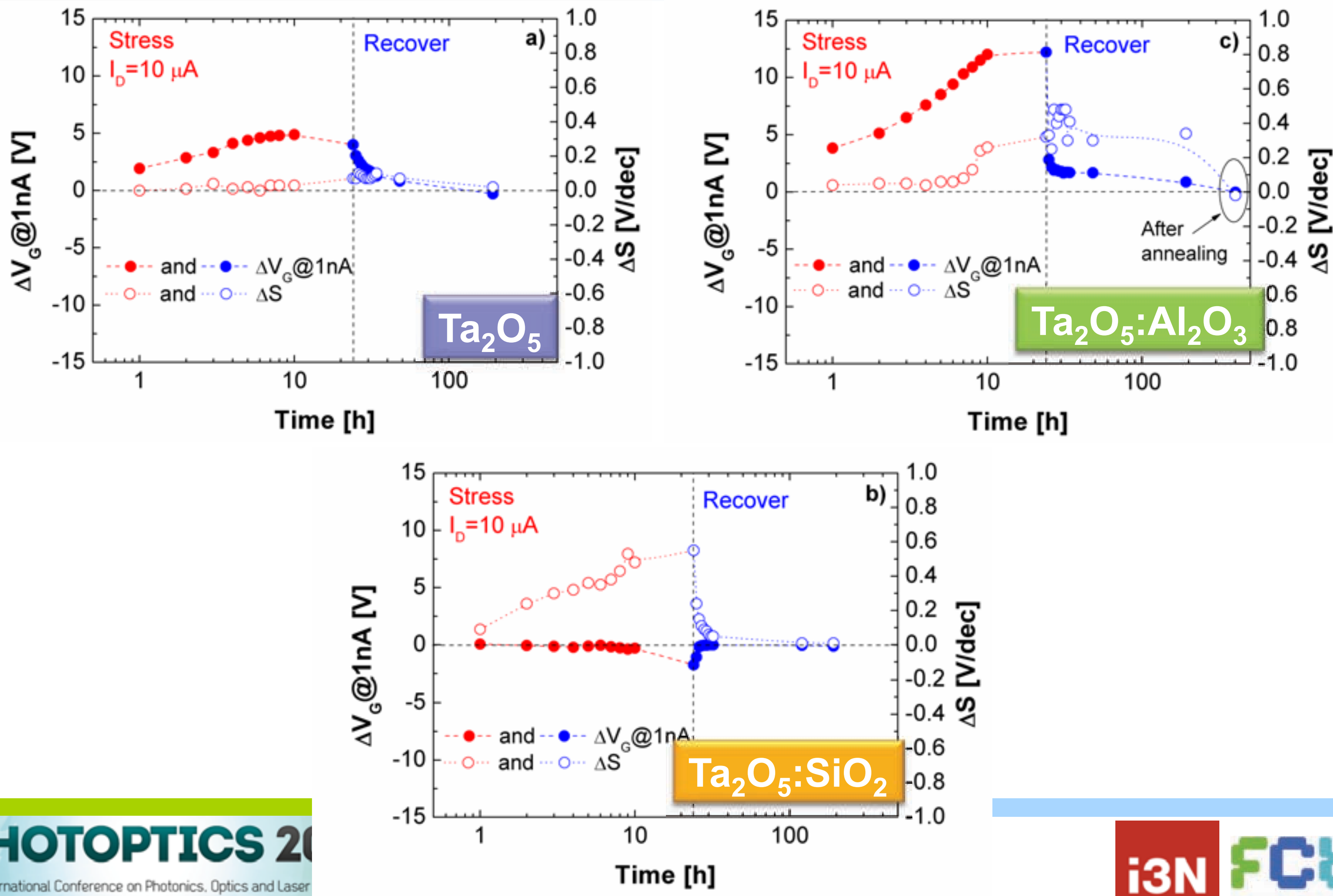
SiO_2

Al_2O_3

Amorphous Multicomponent Dielectrics
AMD *vs* AOS

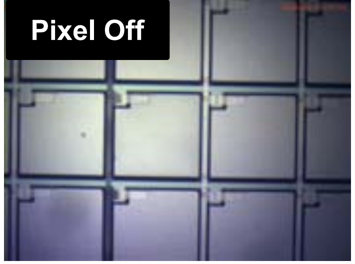
- Stabilization of an amorphous structure
- Increase the band gap

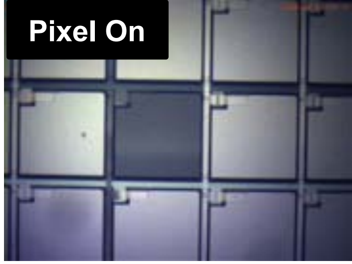
Dielectrics in GIZO TFTs



a-GIZO AMLCD

SIXTH FRAMEWORK PROGRAMME



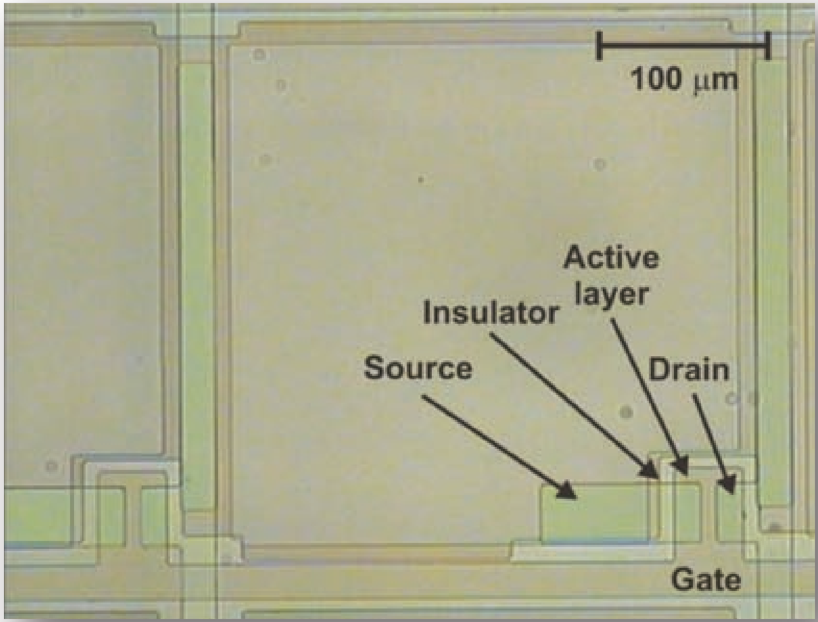


Backplane:

- 5 mask process
- 128x128 pixels, 2.8” diagonal
- Dielectric: co-sputtered Ta_2O_5-SiO_2

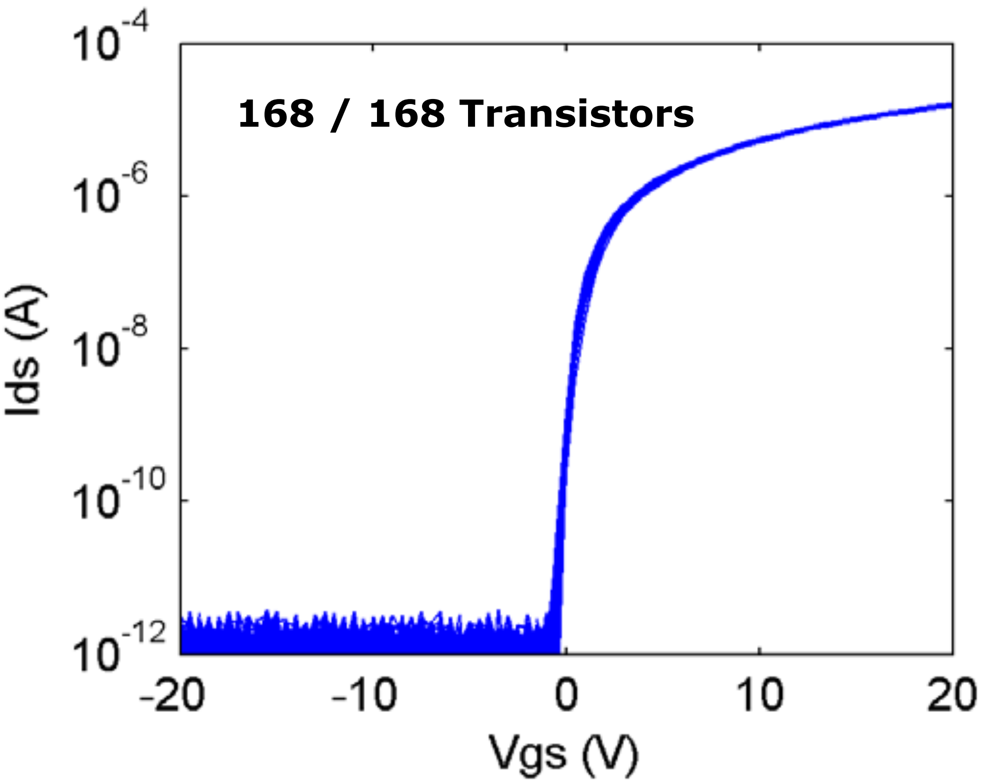
Frontplane:

- Reflective LCD
- White Taylor Guest Host Mode
- Integration by HP @ Bristol/ Dublin



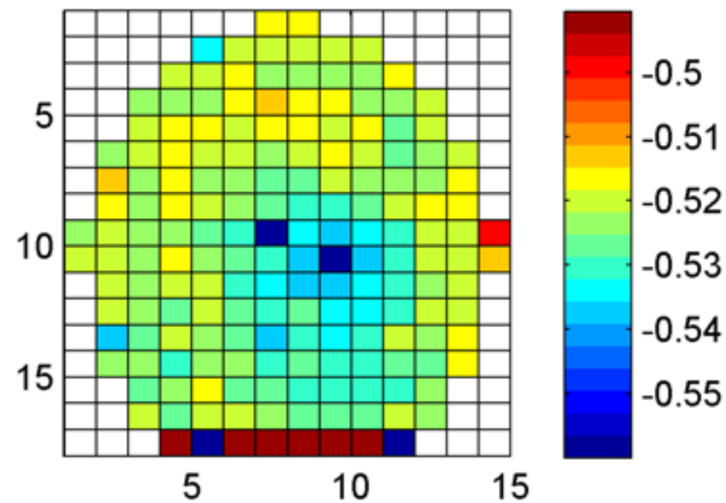
Backplane development: IGZO TFTs on glass

- Mobility ~18 cm^2/Vs
- Excellent uniformity

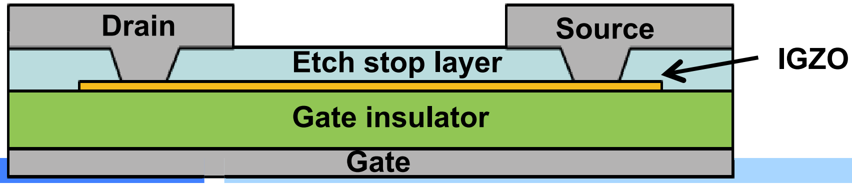


250°C gate insulator
165°C post-fabrication anneal in N_2 oven

Onset Voltage



	Mean	Std	
I_{on}	14.22	0.22	uA
V_{on}	-0.53	0.02	V
mob	18.28	0.42	cm²/Vs

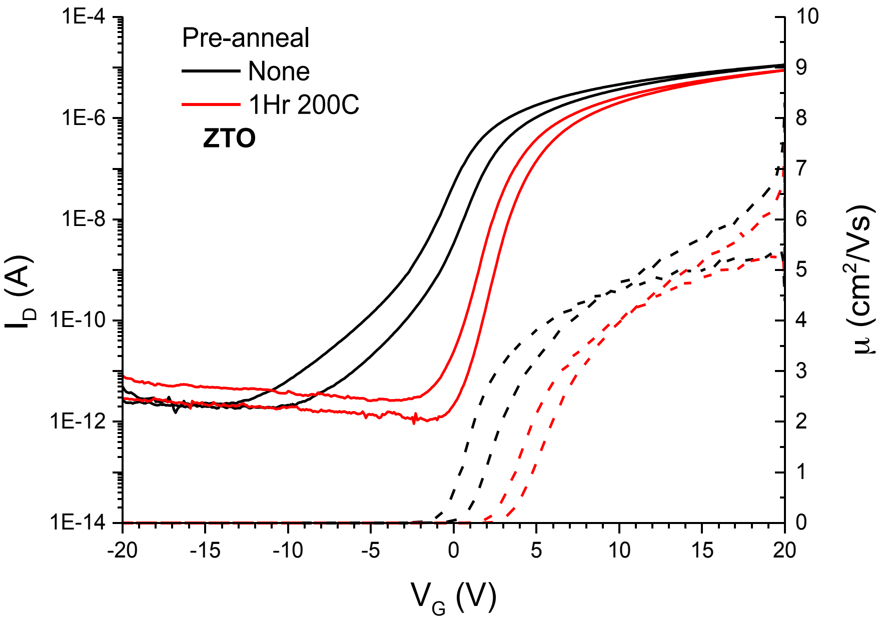


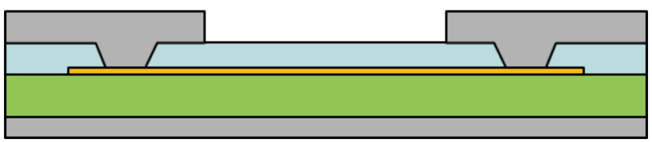
ZTO in PEN-compatible process

ORAMA

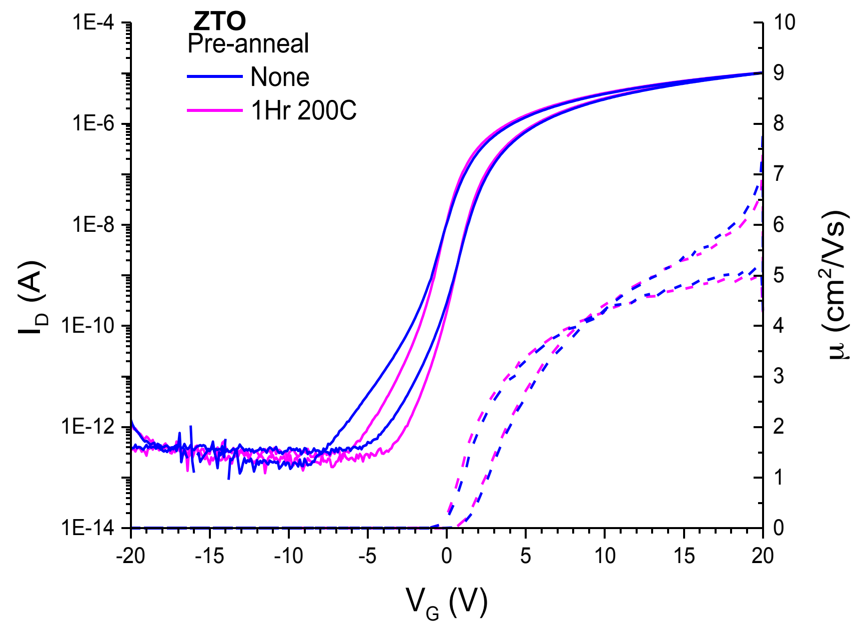
TNO innovation for life

1 hr post-fabrication anneal





4 hr post-fabrication anneal



Mobilities as expected for <200°C process

180°C gate insulator
165°C Post-fabrication anneal in N_2 oven

Display Demo using PVD on Flexible Substrates

IGZO Displays **QQVGA displays**

Gray level control possible

Debonded flexible display

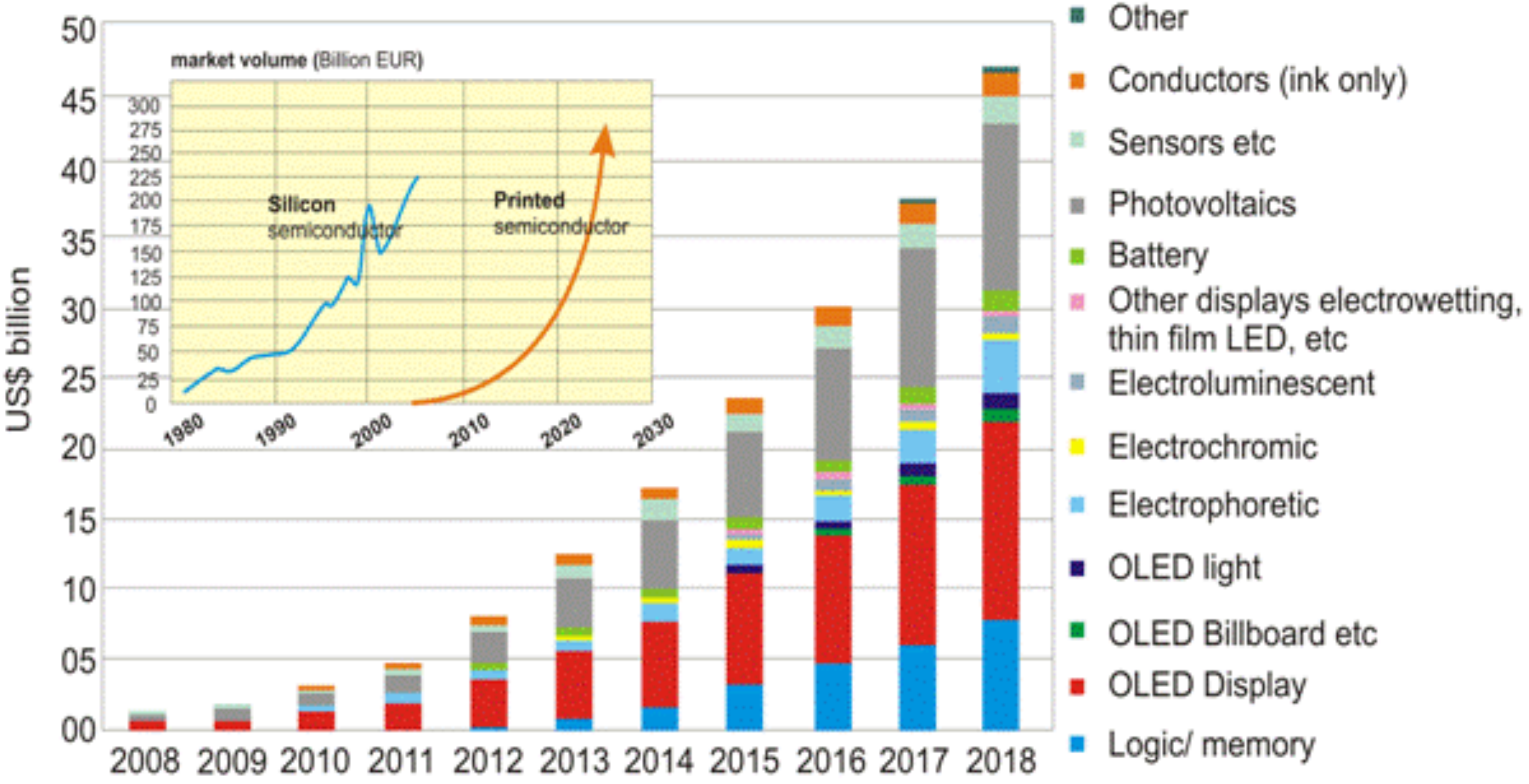
IGZO backplane on PEN

Display Demo Status Overview

Diagonal	4.0 inch	1.0 inch	0.5 inch
Rows x Columns	120x160	120x160	64x160
Pixel Size	300 μm x 300 μm	127 μm x 127 μm	80 μm x 80 μm
Resolution	85 ppi	200 ppi	320 ppi
Pixel Circuit	2T + 1C	2T + 1C	2T+1C, integrated row driver
OLED Structure	Top-Emission	Top-Emission	Top-Emission
Substrate	PEN	PEN	PEN

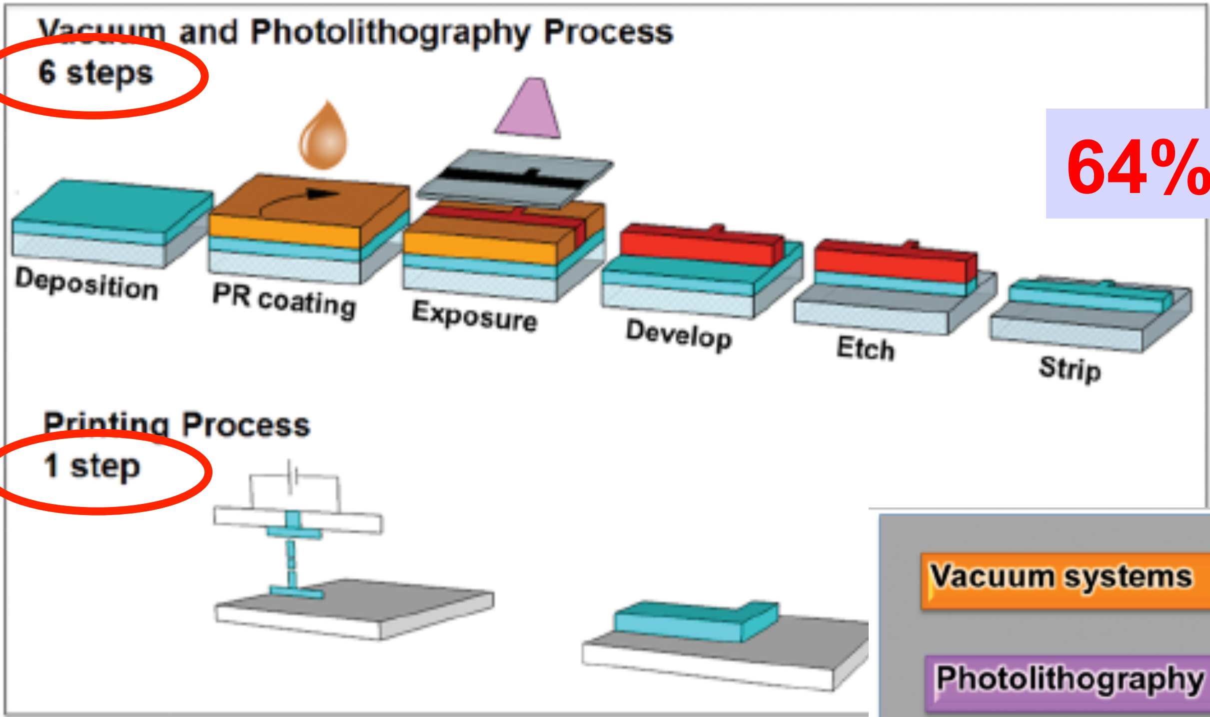
n-type TFTs
Solution-based

Printed electronics

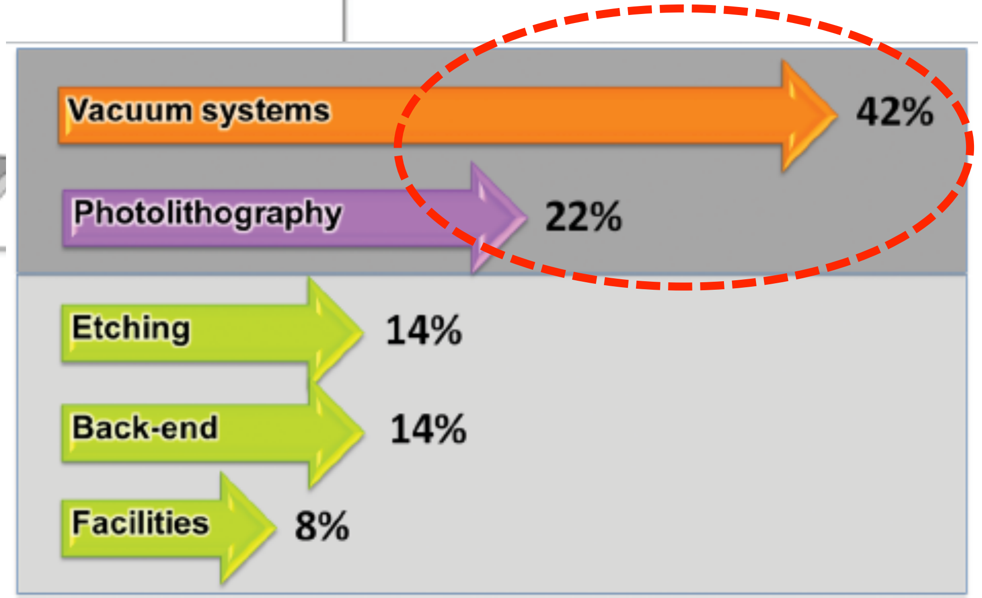


Source: IdTechEx

Needs for cost reduction

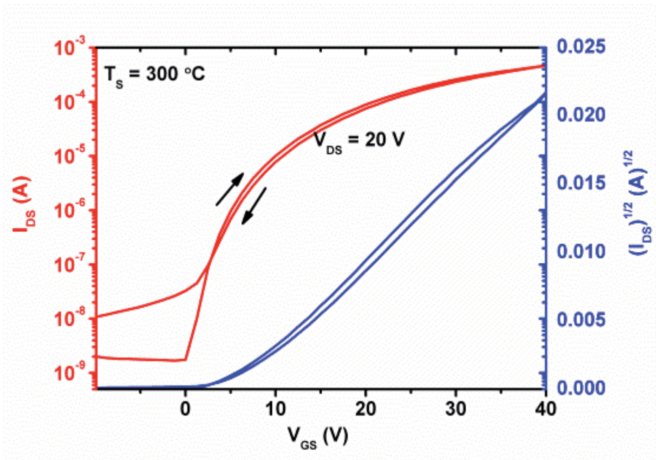


64% cost reduction!!!



Solution processed n-type oxide TFTs – on ITO/ATO

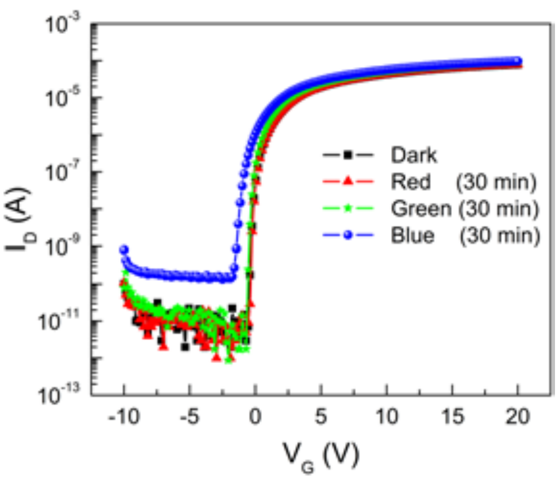
ZTO by spray-pyrolysis, T_{dep}=300 °C



μ_{FE}≈1 cm^2/Vs
On/Off≈10^5
V_{on}≈0 V
S ≈0.6 V/dec

Shanmugan *et al.* JDT (2013)

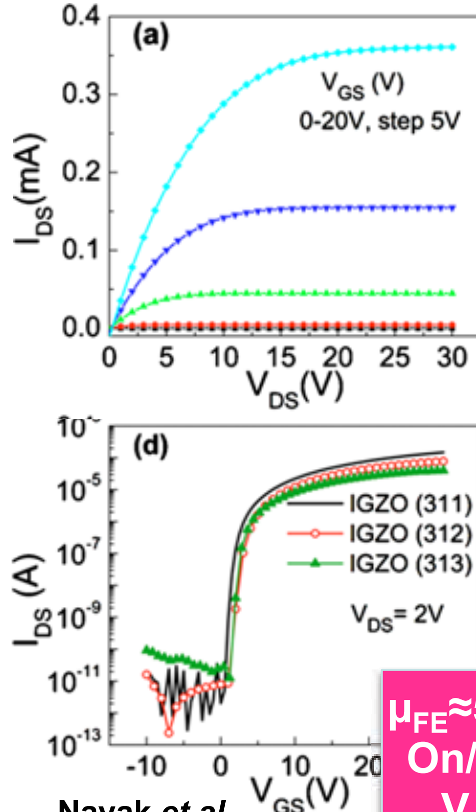
ZTO by spin-coating, T_A=500 °C



μ_{FE}≈5 cm^2/Vs
On/Off≈10^8
V_{on}=-0.9 V
S ≈0.2 V/dec

Nayak *et al.*, JDT 7, 640 (2011)

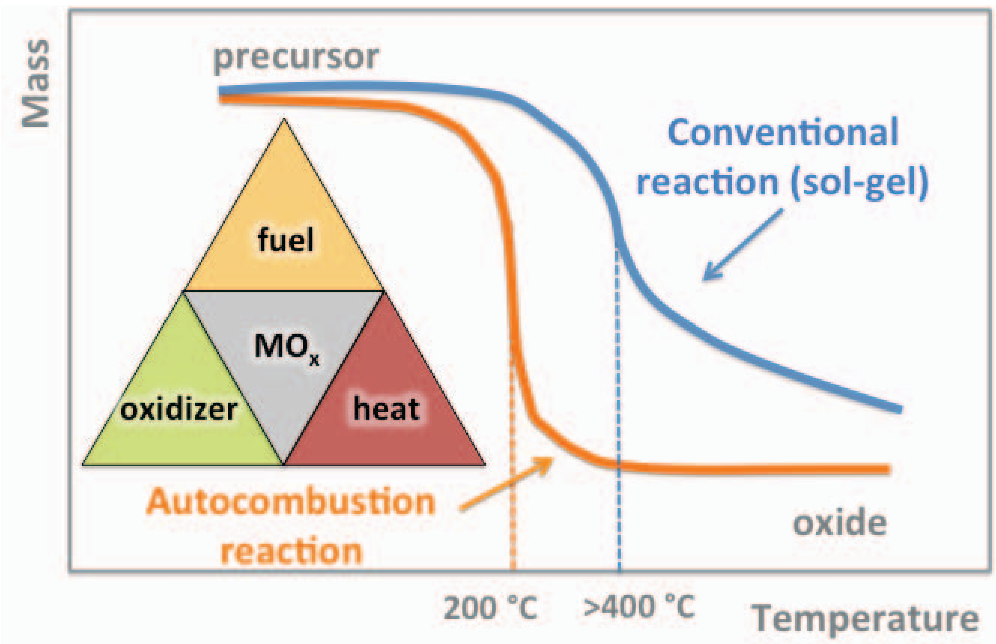
GIZO by spin-coating, T_A=400 °C



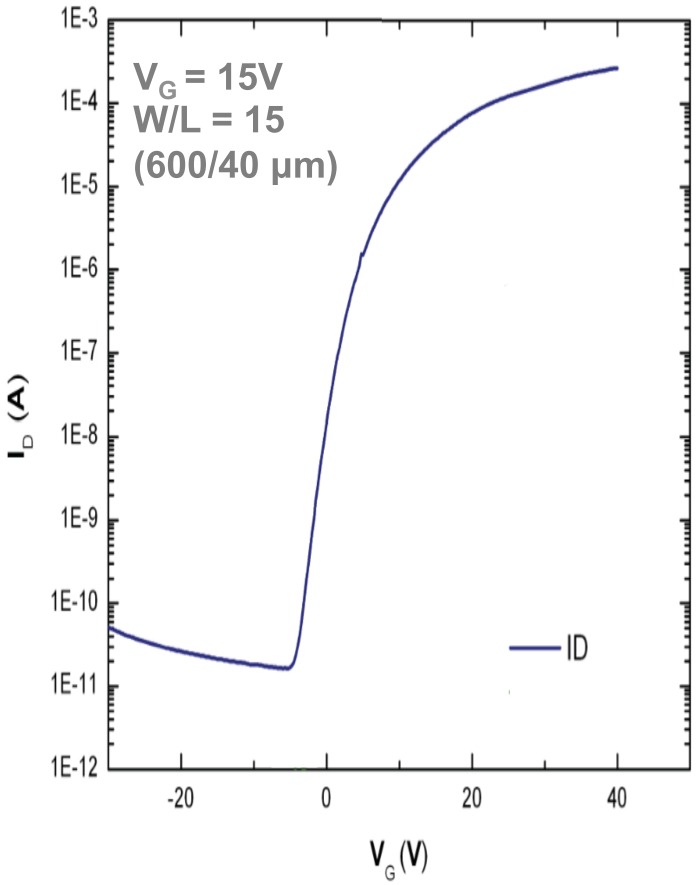
Nayak *et al.*, APL 97 183504 (2010)

μ_{FE}≈5 cm^2/Vs
On/Off≈10^7
V_{on}≈0 V
S=0.28 V/dec

GZTO TFTs (combustion) on ITO/ATO



$I_{on}/I_{off} = 10^7$
$\mu = 6\ cm^2/Vs$



Ga:Zn:Sn = 2:1:0.1 in Methoxyethanol @ 250 ºC

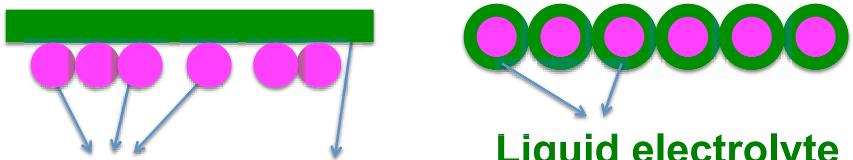
n-type TFTs
MO nanoparticles
(electrolyte-gated)

Electrolyte gated NPs TFTs

ZnO NPs

Dielectric interface

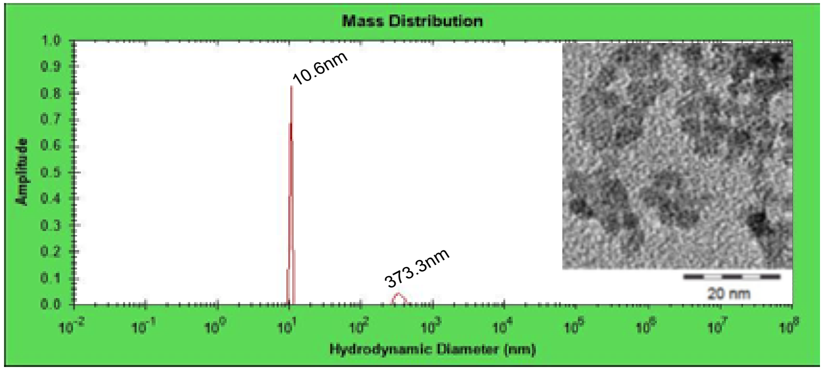
Conventional dielectric | **Gate electrolyte**



Metal oxide nanoparticles

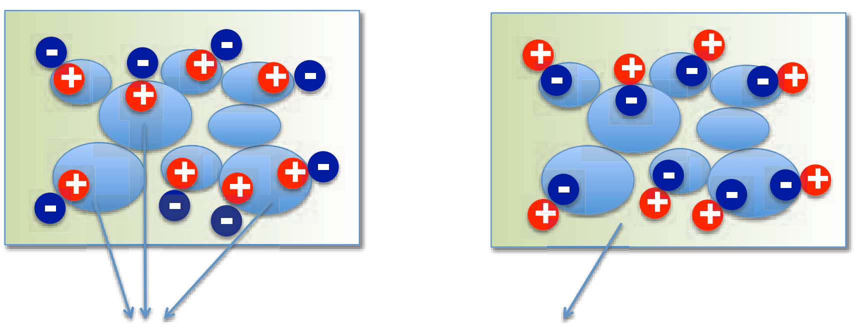
Dielectric thin film

Liquid electrolyte
(after drying becomes solid)



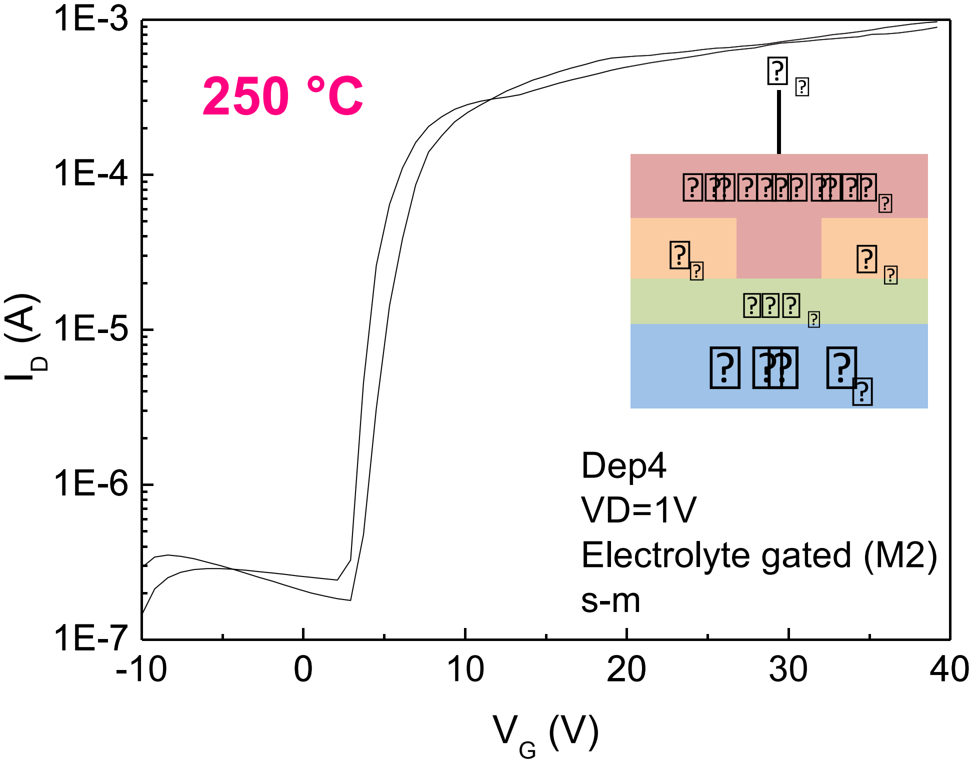
Device working principle
(interface electrolyte-channel layer)

OFF-state (V_G<0 V) | **ON-state** (V_G>0 V)



Channel n-type nanoparticles

Electrolyte

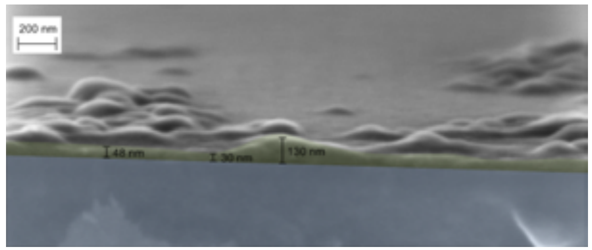


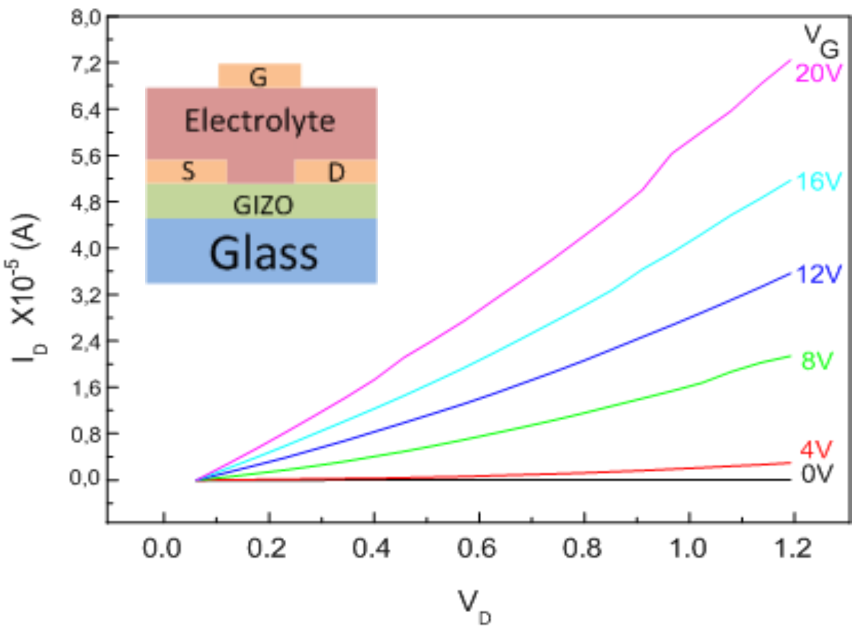
Electrolyte gated NPs GIZO TFTs

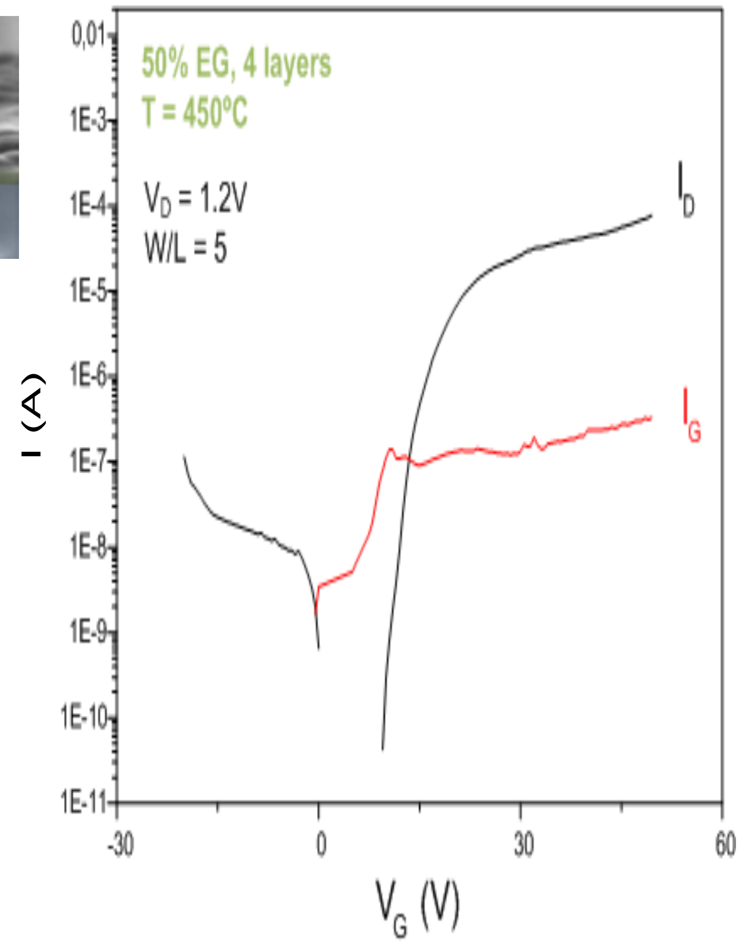
$I_{ON}/I_{OFF} = 4 \times 10^6$

$V_T = 13\ V$

$\mu_{SAT} \approx 0.1\ cm^2/Vs$

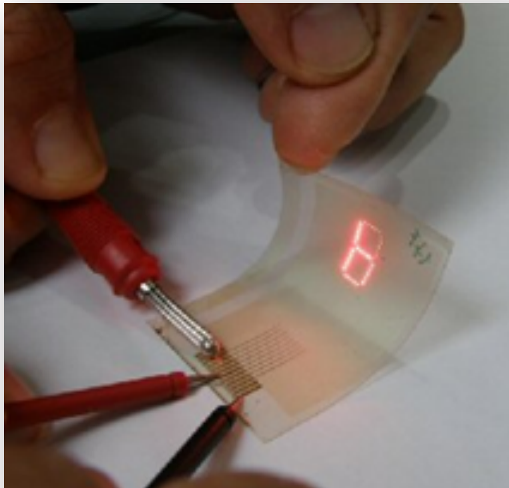


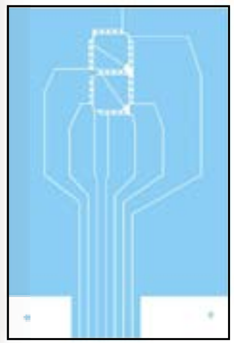




Passive and active matrix backplanes

IZO electrodes as a passive matrix for chipLED



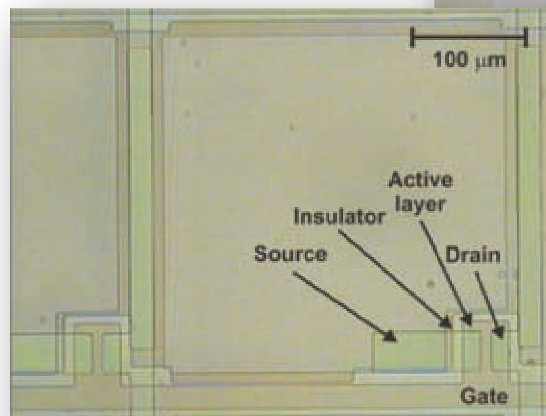


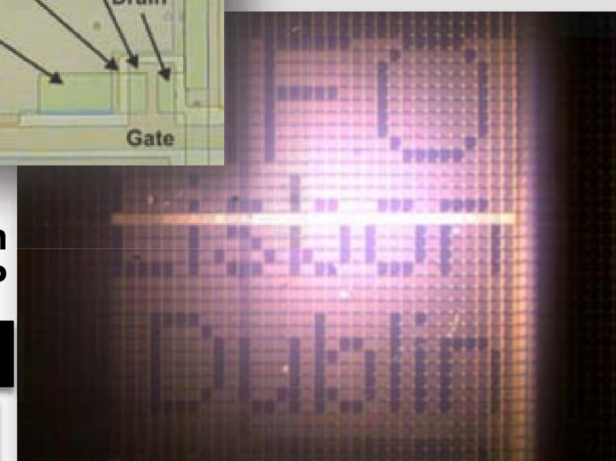
- Alphanumeric, 7 segments
- For HUD application in automotive industry

Collaboration with Centro Ricerche Fiat (CRF)

GIZO TFTs for active matrix of LCD display

- Resolution: 128x128
- Pixel area: 350µm x 350 µm
- 5 mask process





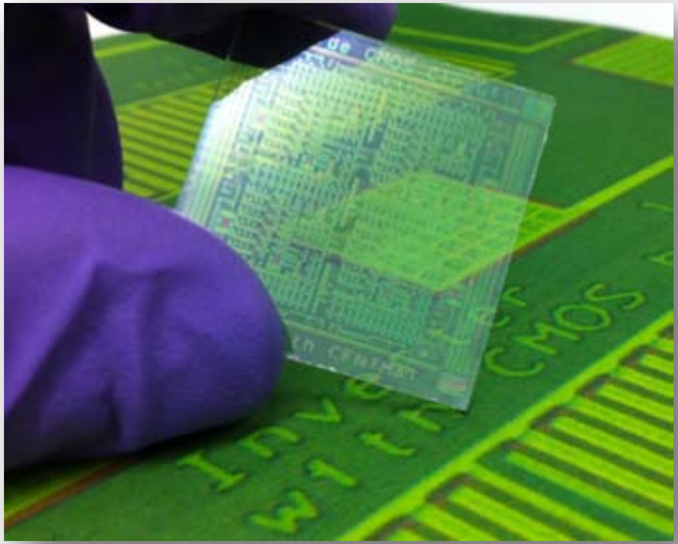
Collaboration with HP

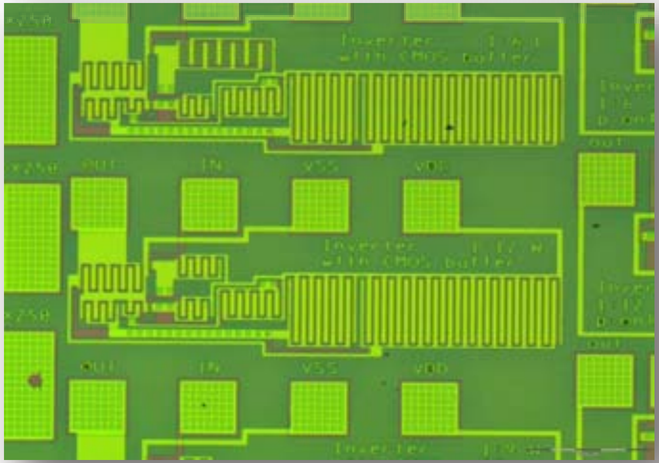
In the framework of Multiflexioxides FP6 project

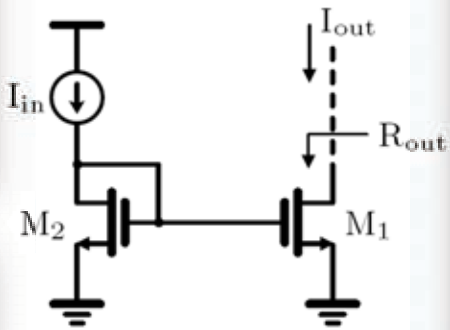
Material/devices properties significantly enhancecd from then...

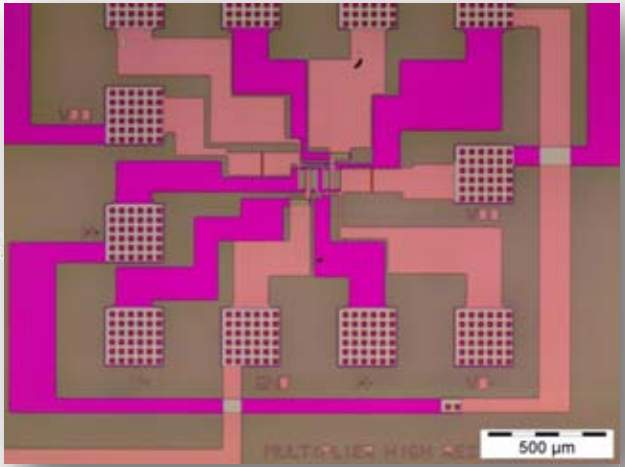
Transparent circuits

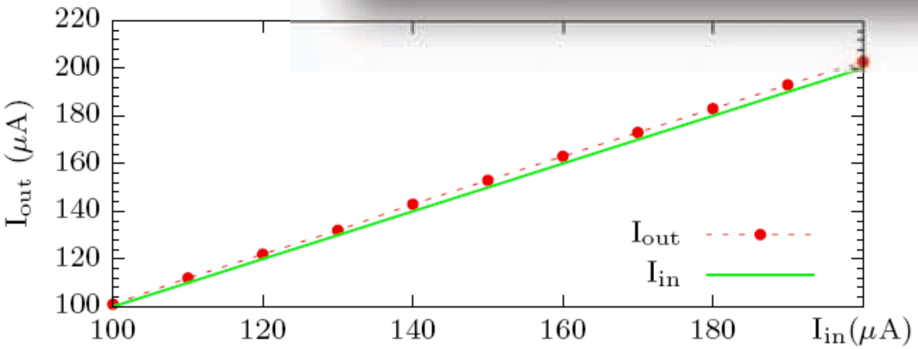
- Using n-MOS technology (GIZO for now) and multilayer/multicomponent dielectrics
- Simple transparent circuits such as inverters, current mirrors, multipliers, with T_{MAX}=150 °C
- Complete characterization underway...



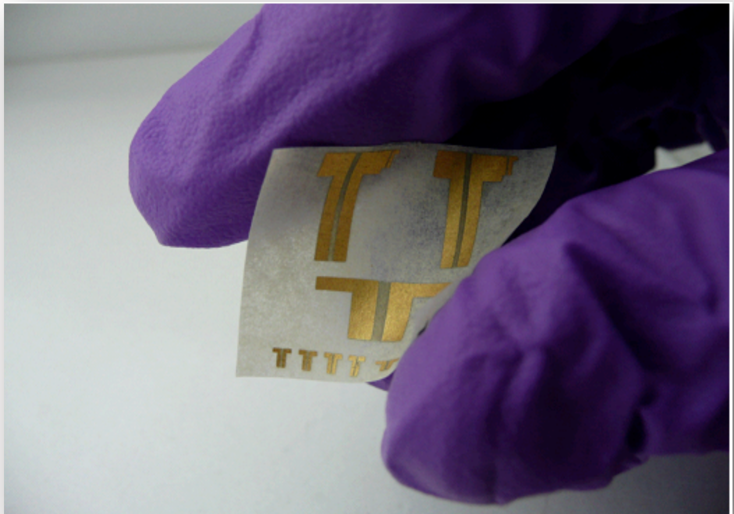




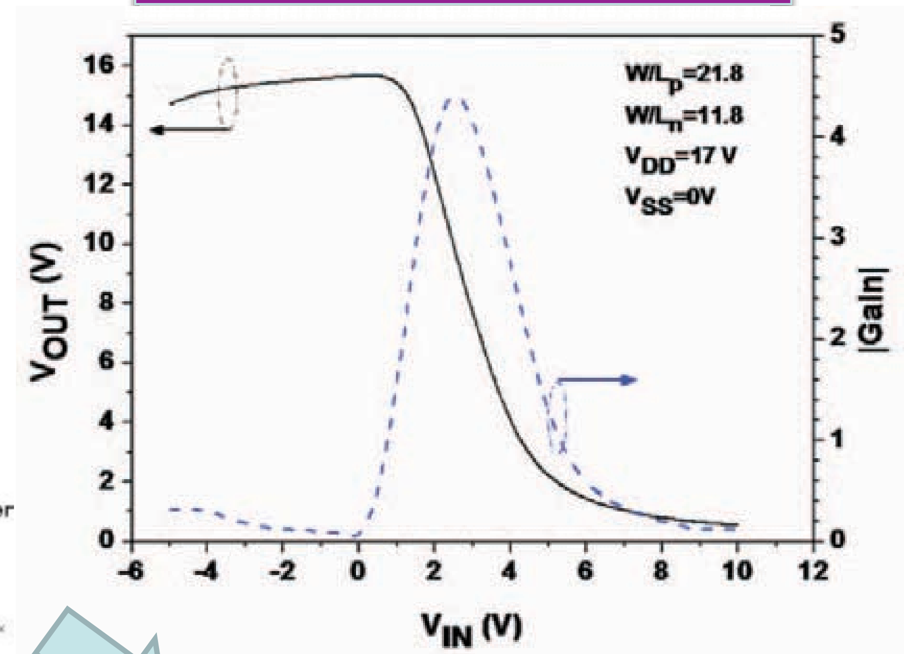


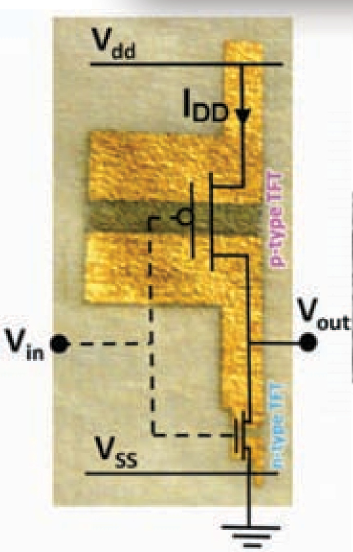


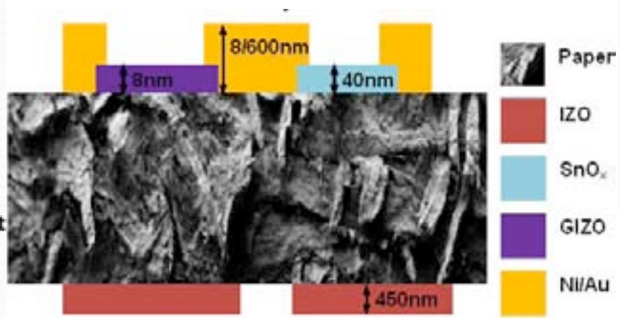
Paper electronics (Paper-e®)



- Even CMOS with GIZO and SnO already possible...
- ...even with paper.

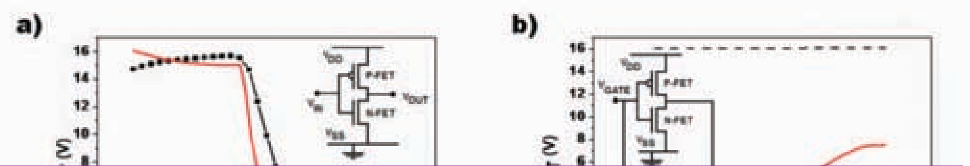






Towards low-cost, recyclable electronics

Logic circuits on/with paper



Recyclable, Flexible, Low-Power Oxide Electronics

Rodrigo F. P. Martins[1,*], Arman Ahnood[2], Nuno Correia[1], Luís M. N. P. Pereira[1], Raquel Barros[1], Pedro M. C. B. Barquinha[1], Ricardo Costa[1], Isabel M. M. Ferreira[1], Arokia Nathan[2,*], Elvira E. M. C. Fortunato [1,*]

Article first published online: 29 NOV 2012

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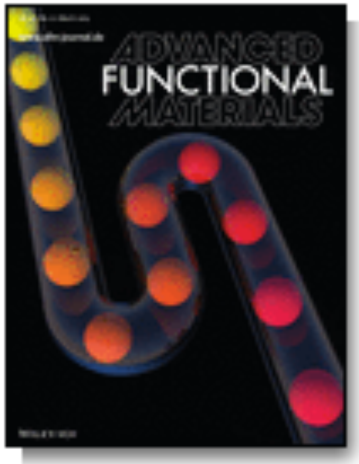
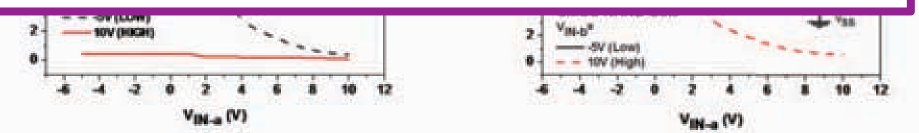
Issue



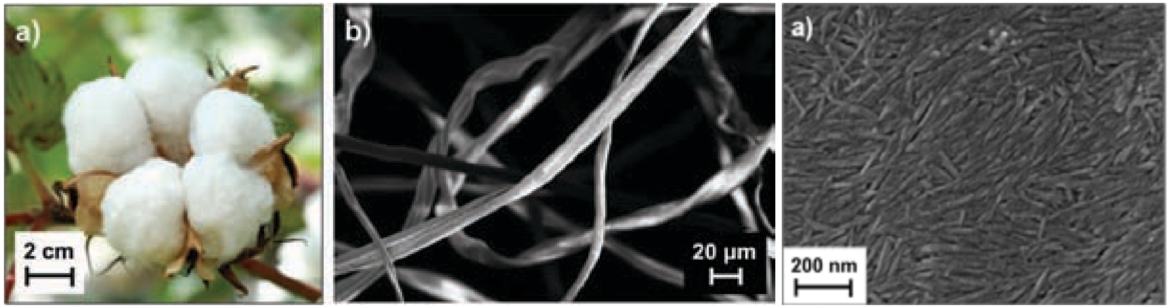
Advanced Functional Materials

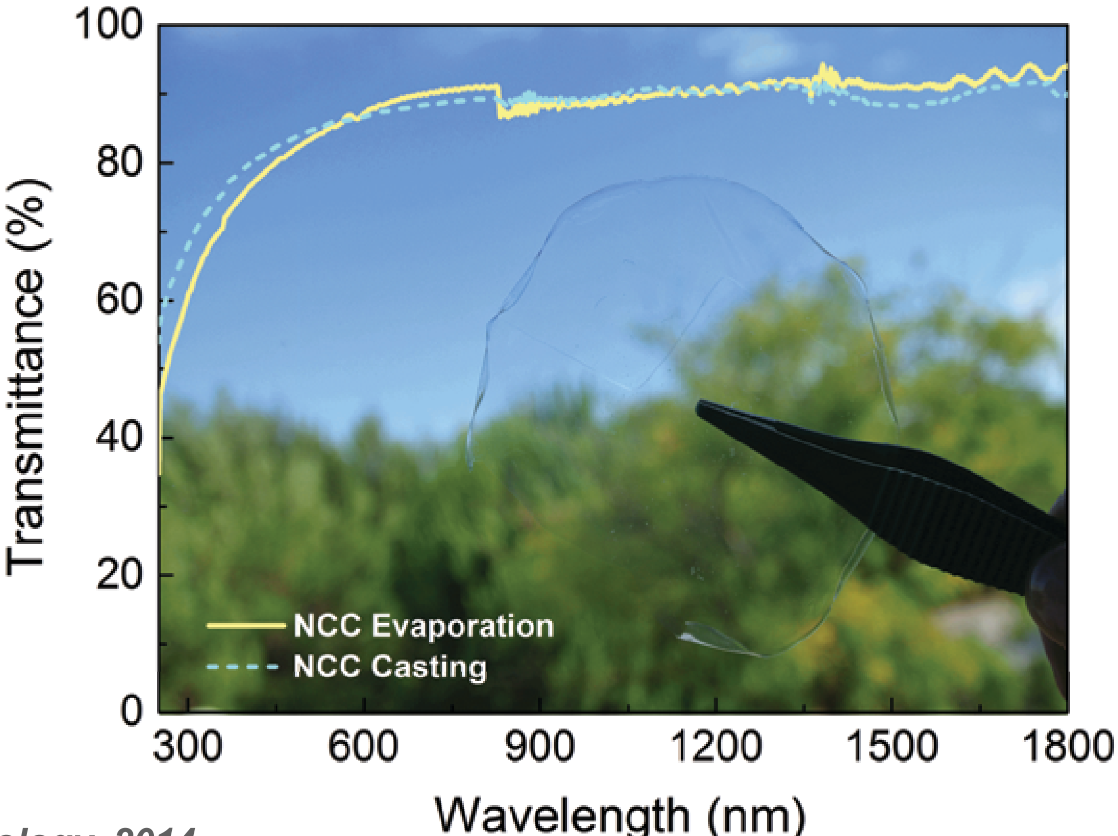
Volume 23, Issue 17, pages 2153–2161, May 6, 2013



R. Martins et al., Adv. Func. Mat. 201202907, 2012

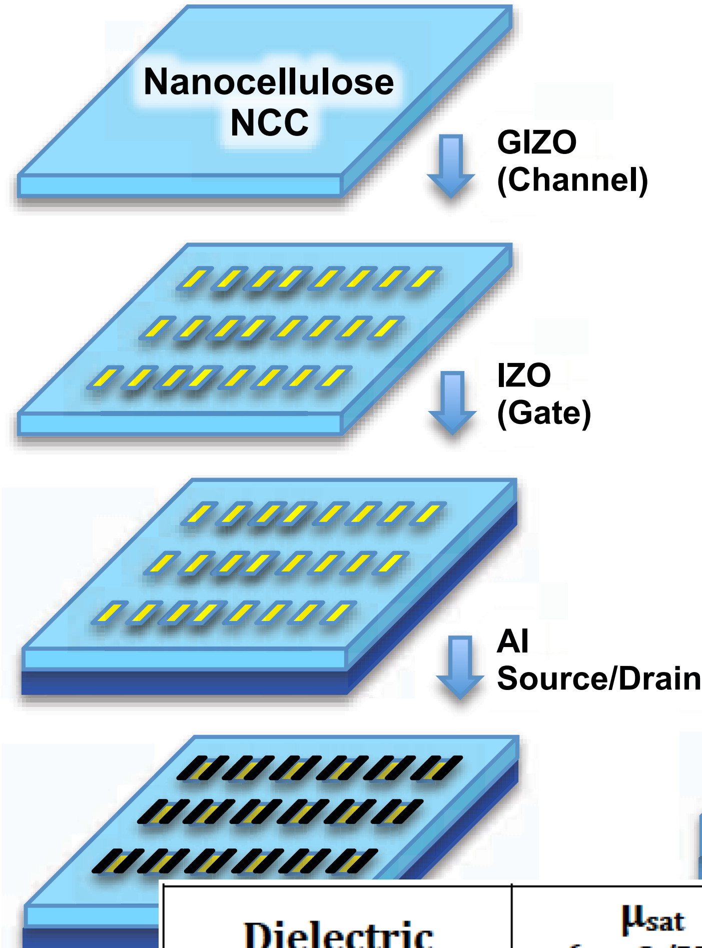
Nanopaper
(cotton fibers)

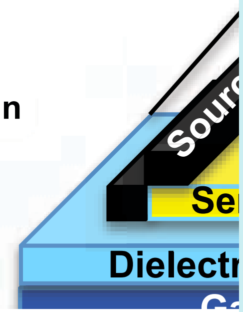


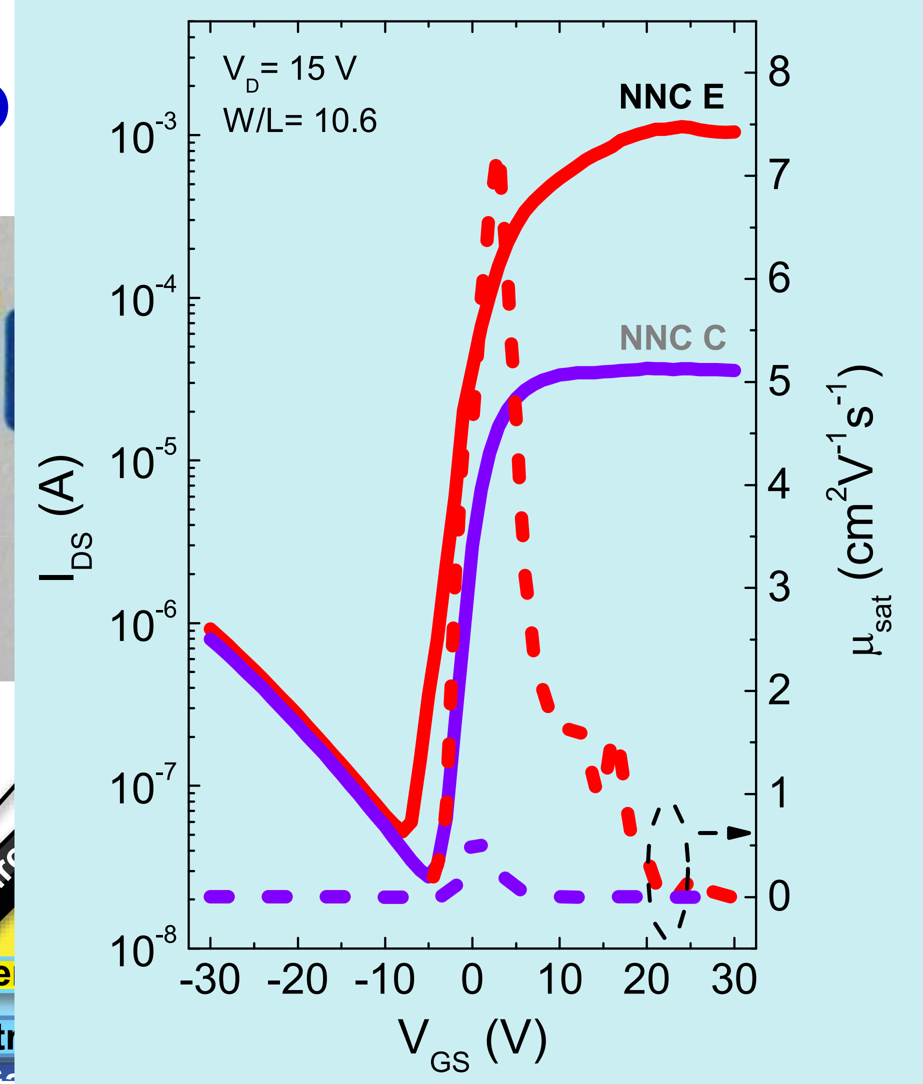


Accepted Nanotechnology, 2014

Nanopaper transisto







Dielectric	μ_{sat} (cm^2/Vs)	V_{ON} (V)	I_{ON}/I_{OFF}	S (V/dec)
NCC evaporation	7.27	-8	2×10^5	2.11
NCC casting	0.54	-5	1×10^4	1.79

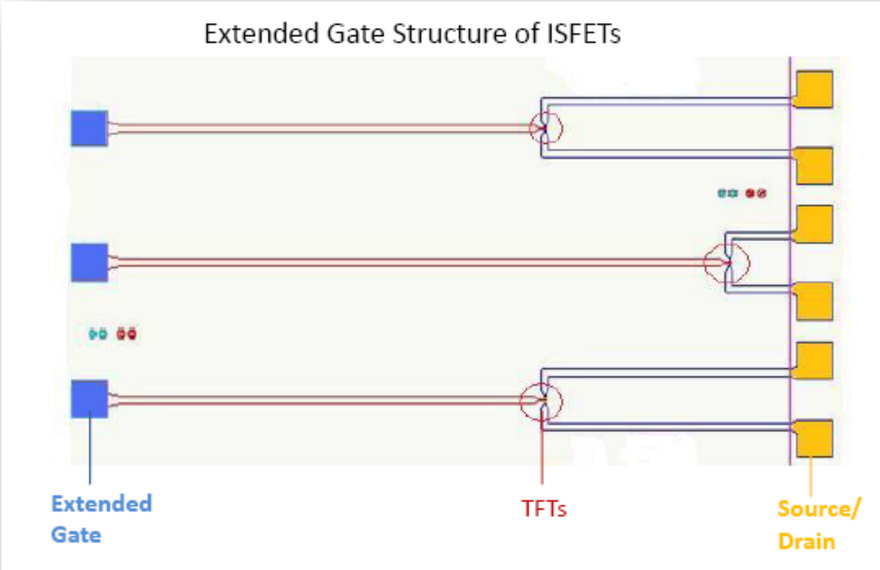
General conclusions

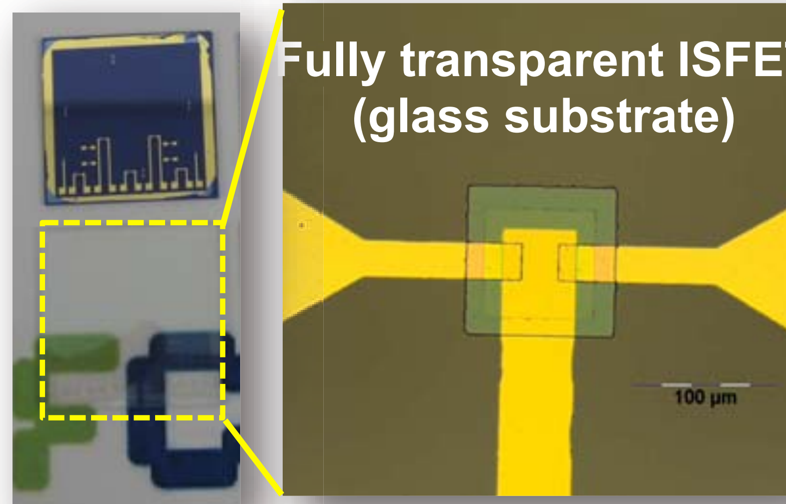
Amorphous structure	→	Large area uniformity
Superior performances	→	High mobility
Transparency	→	Specific applications
Stability	→	Aging effects not existing
Electrical stability	→	No current bias stress
Passivation	→	Already achieved
Simple structure	→	Reduced process steps, no need of n^+ contacts

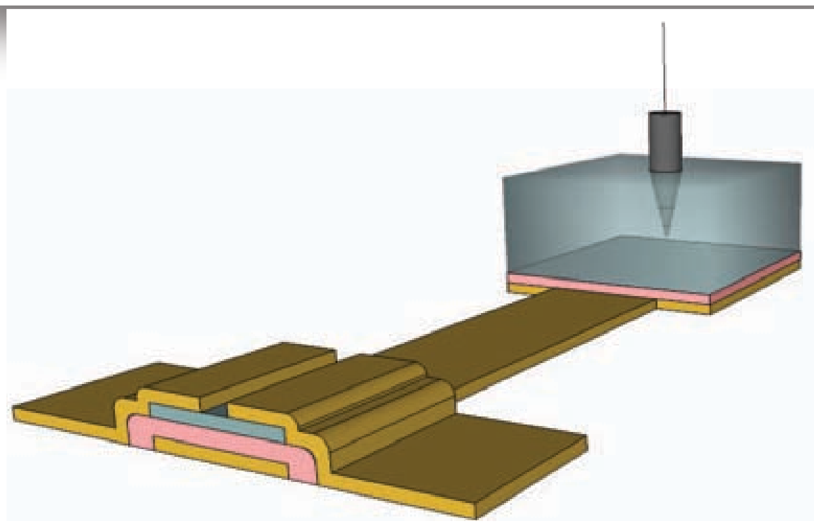
Ideal oxide material for TFT appication:

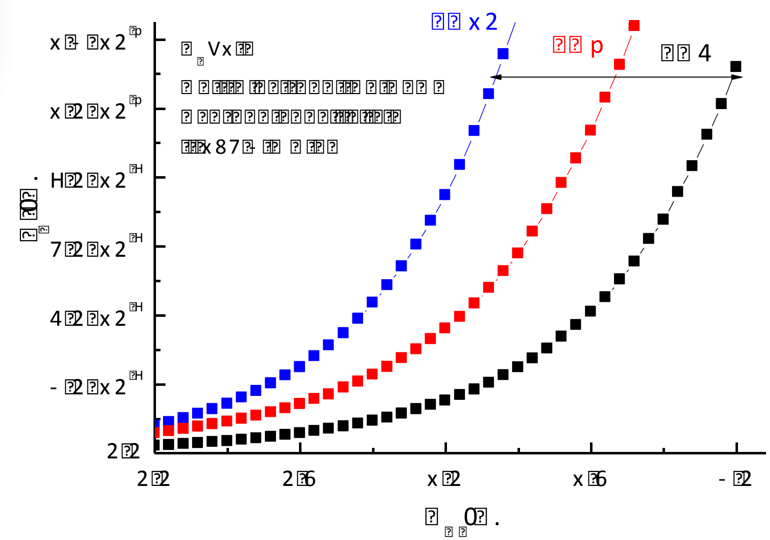
- high carrier mobility
- low carrier concentration
- non-vacuum deposition
- low temperature deposition

Biosensors / ISFETs









R. Branquinho et al., Biosensors & Bioelectronics, 28 (2011), 44.
J. Pinto *et al*, JDT (2013) accepted

All Oxide
Solar Cells

http://alloxidepv.eu/

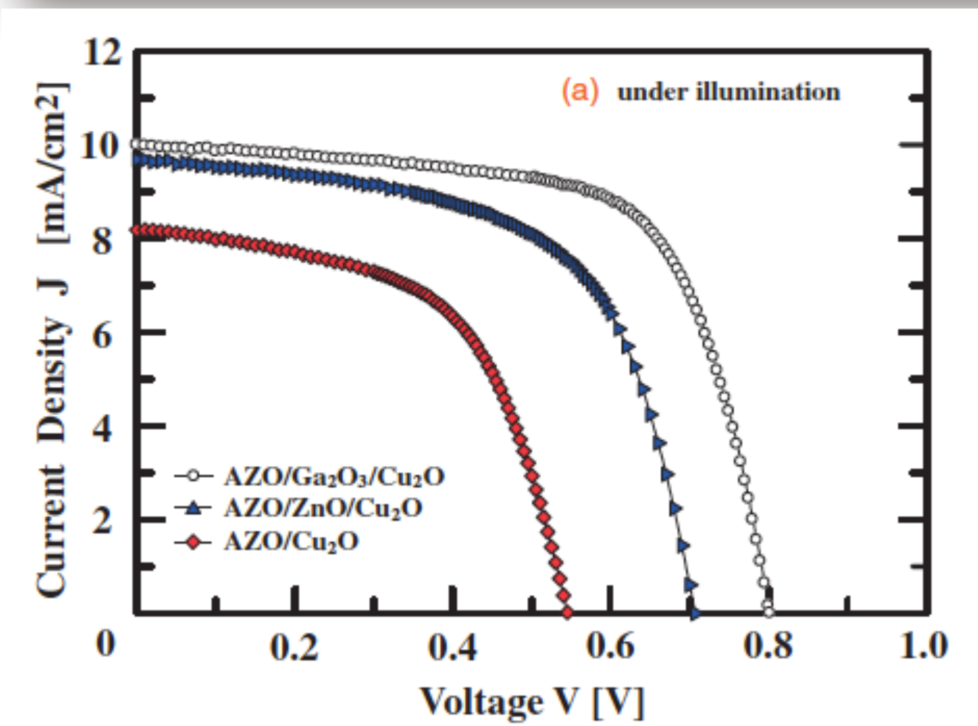
Applied Physics Express 6 (2013) 044101
http://dx.doi.org/10.7567/APEX.6.044101

High-Efficiency Cu_2O-Based Heterojunction Solar Cells Fabricated Using a Ga_2O_3 Thin Film as N-Type Layer

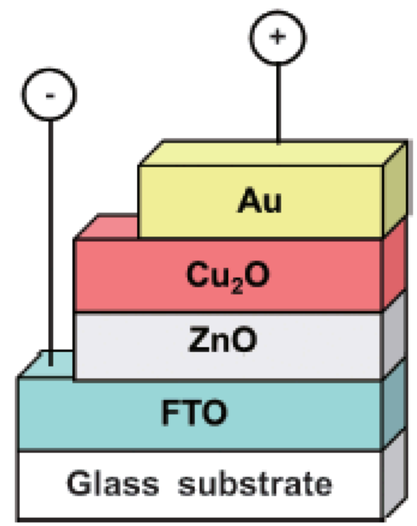
Tadatsugu Minami, Yuki Nishi, and Toshihiro Miyata

Optoelectronic Device System R&D Center, Kanazawa Institute of Technology, Nonoichi, Ishikawa 921-8501, Japan

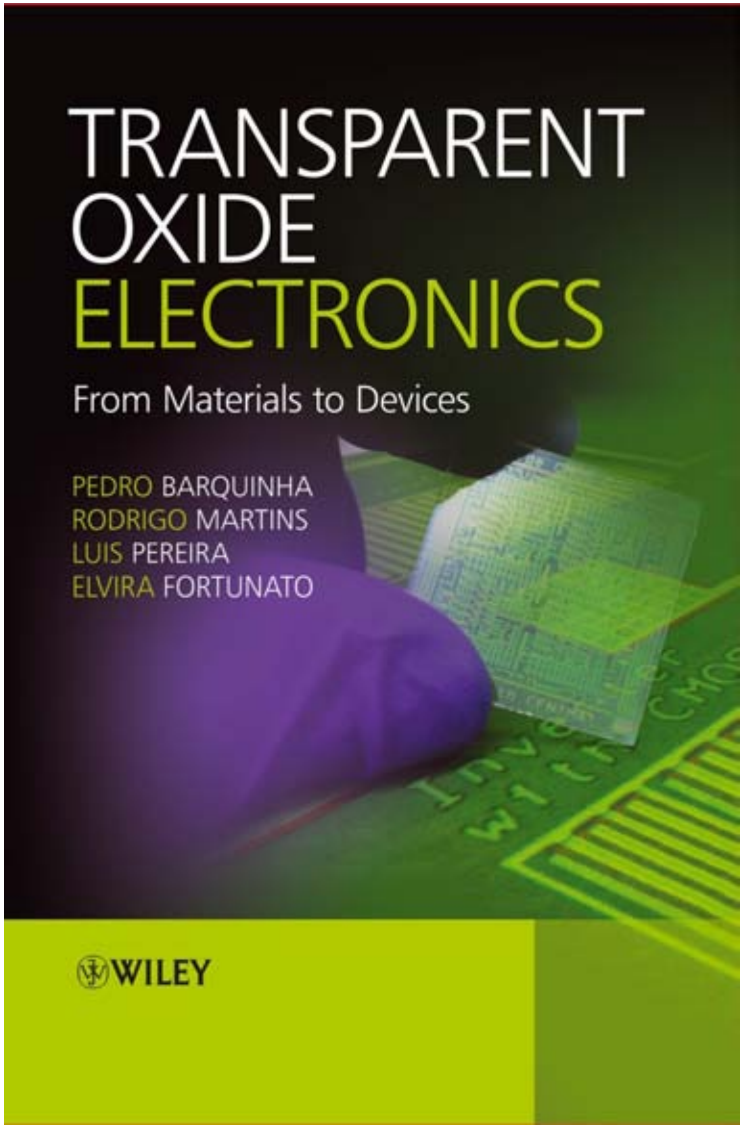
Received January 16, 2013; accepted March 7, 2013; published online March 27, 2013



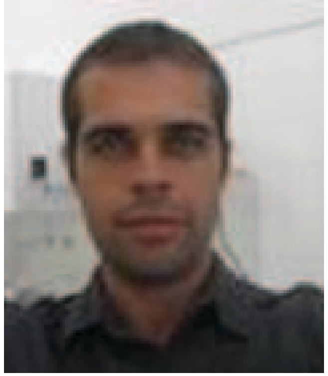
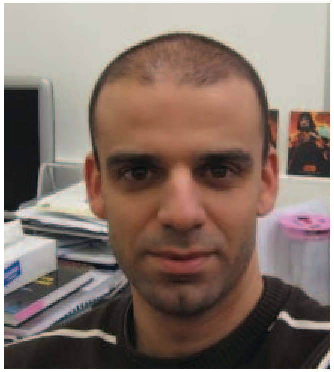
The highest efficiency of **5.38%** was obtained in an Al-doped ZnO/ nondoped Ga_2O_3/Cu_2O heterojunction solar cell.



Further reading...





2012

- **N-type TOS**
- **P-type TOS**
- **Gate dielectrics in oxide electronics**
- **The (r)evolution of TFTs**
- **Electronics with and on paper**
- **Current and upcoming applications**

“INVISIBLE”
(ERC-2008-AdG 228144)

Thank you for your attention!

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